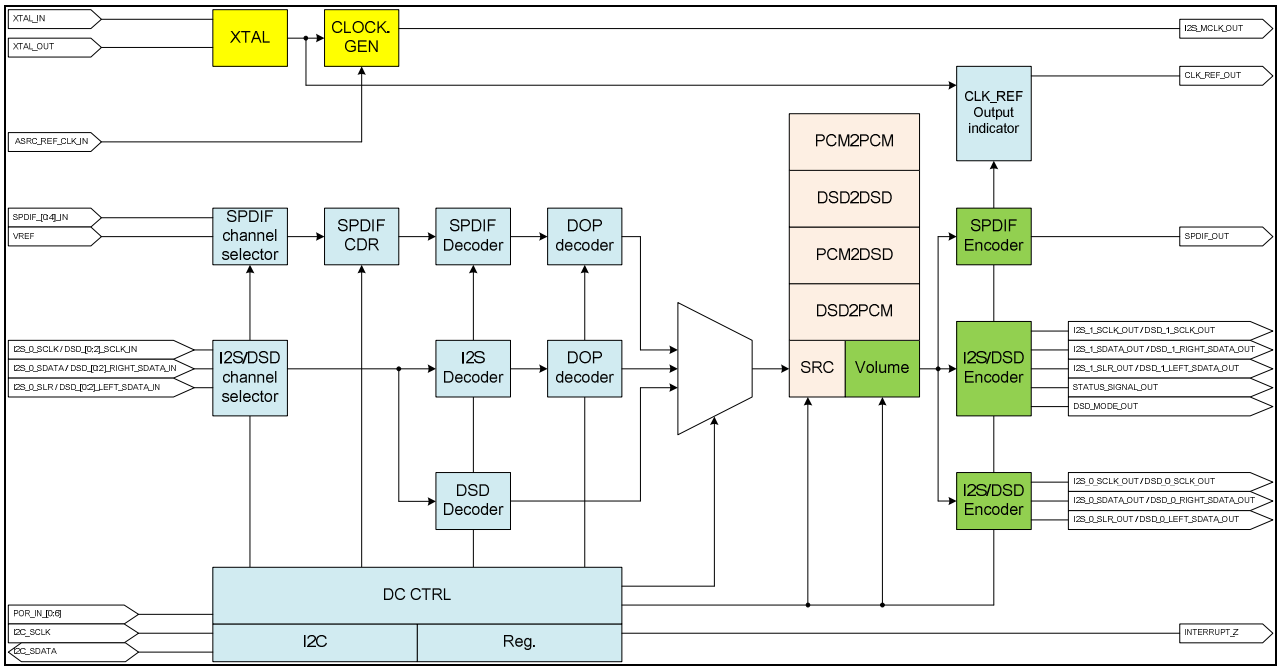
General Description

The CT7302/CT5302 is a single chip dual channel audio digital to digital bridge with sample rate converter. The chip also provides System Management Bus 1.0 (also refer the I^{2}C specification) for programming device function.
In all system application, I2C configure is needed. Power on initial is mute.

Features

- SPDIF support up to 768 KHz / 32 bits mode.
- I2S support up to 768 KHz / 32 bits mode.
- DSD support 1x/2x/4x/8x mode.
- DoP support 1x/2x/4x mode, through I2S.
- DoP support 1x/2x/4x mode, through SPDIF
- PCM SRC / ASRC fully support 32 KHz ~ 768 KHz.
- PCM / DSD / DoP to PCM / DSD / DoP converter with SRC / ASRC.
- I2S Rx standard / left justified slave mode. I2S Tx standard / left justified master/slave mode.
- Basic auto De-pop function.
- I^{2}C interface. / Interrupt function. / Full function software mode support. / Software Power Down feature.
- Crystal reference clock / MCLK / DoP / Mute status output.
- Auto De-emphasis 32 KHz / 44.1 KHz / 48 KHz.
- Auto detecting PCM / DoP format.
- Auto detecting I2S / DSD interface.
- Volume control with fading in/out. (+18dB ~ -110dB step 1/32 dB)
- SRC / ASRC 32 bits dynamic range (192dB), THD+N (-174dB).



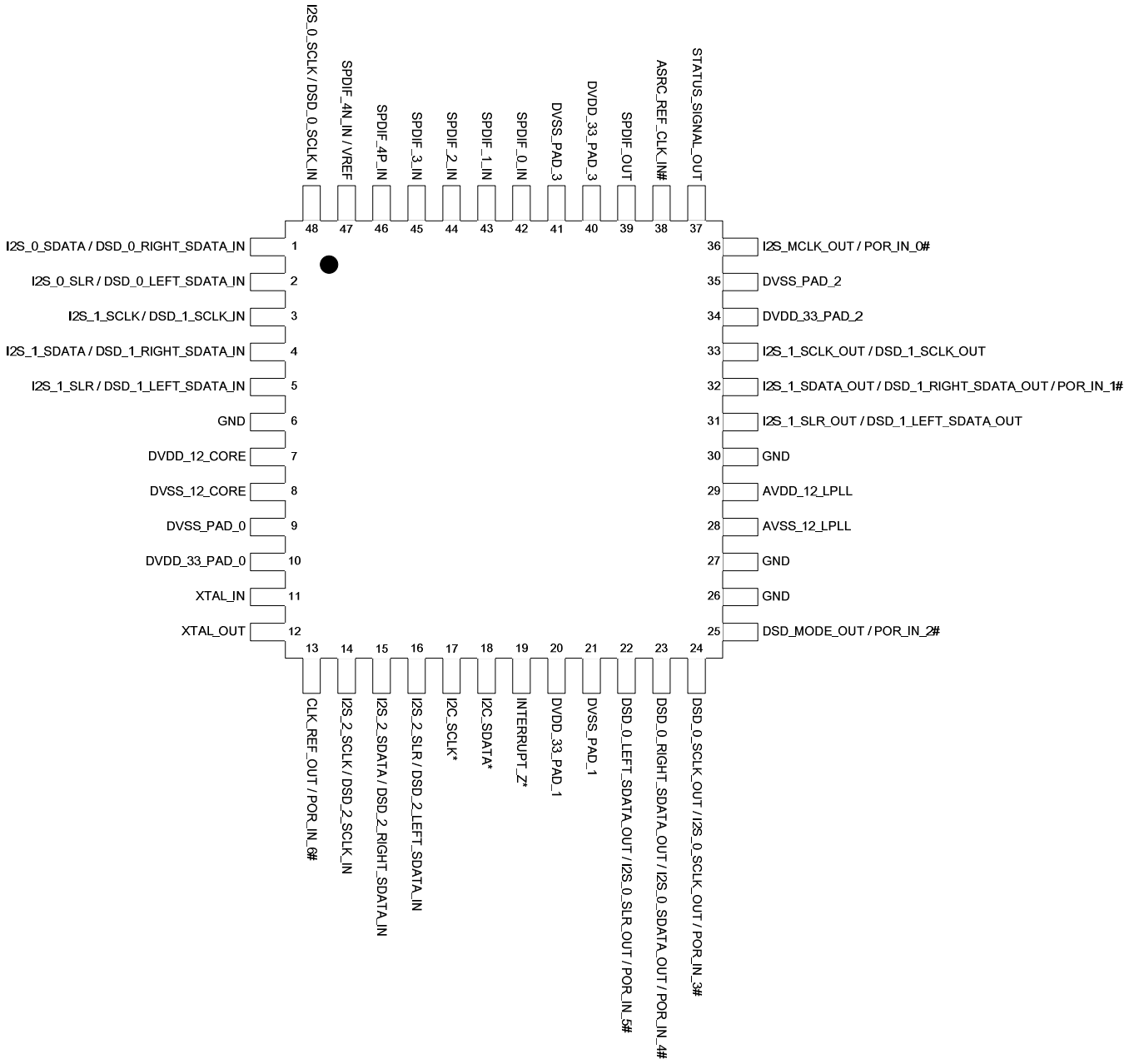
CT7302/CT5302 family

Description	CT7302PL	CT7302CL	CT7302EL	CT7302SL	CT5302SL	CT5302SN
Input Receiver						
I2S / DSD port	3	3	3	3	3	1
I2S	*768kHz / 32-bit	768kHz / 32-bit	768kHz / 32-bit	384kHz / 32-bit	384kHz / 32-bit	384kHz / 32-bit
SPDIF port	5	5	5	5	2	2
SPDIF	768kHz / 32-bit	384kHz / 32-bit	384kHz / 24-bit	192kHz / 24-bit	192kHz / 24-bit	192kHz / 24-bit
DSD	**8x	4x	4x	2x	1x	1x
I2S DoP	4x	4x	4x	2x	1x	1x
SPDIF DoP	4x	2x	2x	1x	1x	1x
Output Transmitter						
I2S / DSD port	2	2	2	2	2	2
I2S	768kHz / 32-bit	768kHz / 32-bit	768kHz / 32-bit	384kHz / 32-bit	384kHz / 32-bit	384kHz / 32-bit
SPDIF port	1	1	1	1	1	1
SPDIF	768kHz / 32-bit	384kHz / 32-bit	384kHz /24-bit	192kHz / 24-bit	192kHz / 24-bit	192kHz / 24-bit
DSD	8x	4x	4x	2x	1x	1x
I2S DoP	4x	4x	4x	2x	1x	1x
SPDIF DoP	4x	2x	2x	1x	1x	1x
DSD/PCM converter						
DSD to PCM **BASIC** SRC	V	V	V	V	V	V
DSD to PCM **Advance** SRC	V	V	V	V	X	X
PCM to DSD	V	V	X	X	X	X
Package						
Package	LQFP 48	LQFP 48	LQFP 48	LQFP 48	LQFP 48	QFN 32

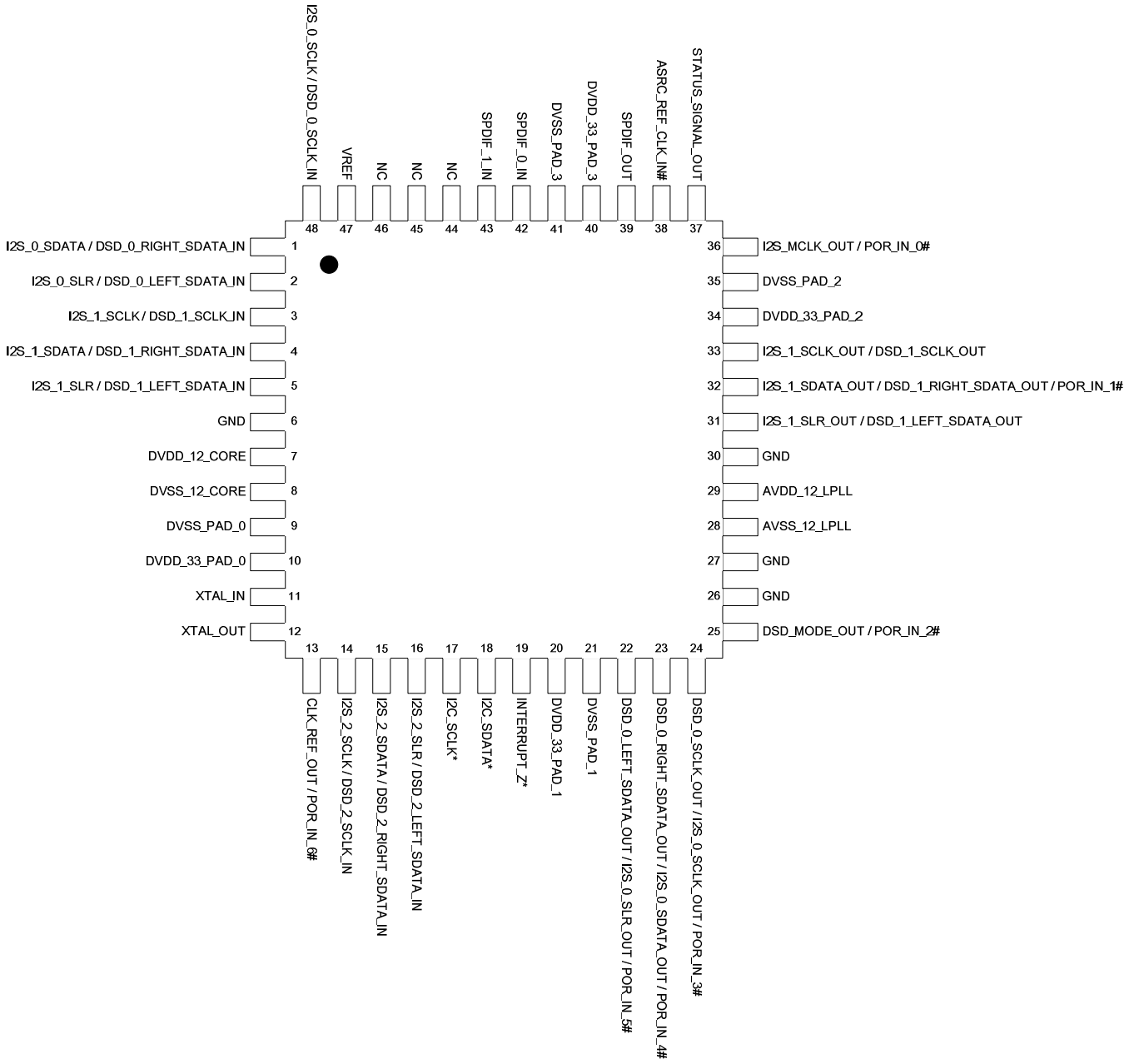
* (768kHz/32-bit : max data rate) means that data rate support from 32kHz/24-bit to 768kHz/32-bit.

** (8x : max data rate) means that data rate support from 1x(64fs) to 8x(512fs). ….. fs = 32kHz/44.1kHz/48kHz

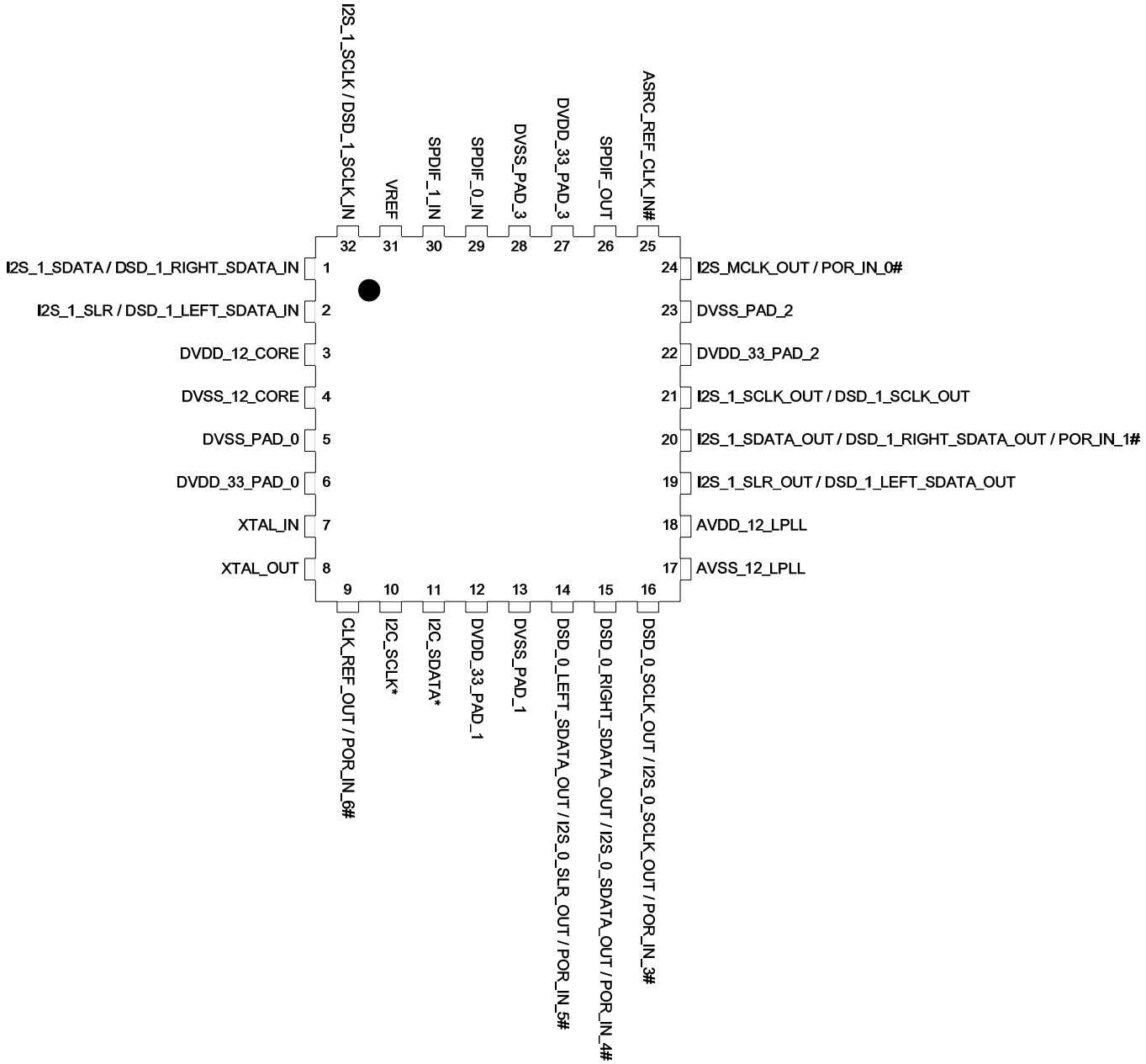
Package LQFP-48 (Top View) CT7302xL



Package LQFP-48 (Top View) CT5302xL



Package QFN-32 (Top View) CT5302xN, CT7302xN



LQFP 48/32 Pin Description

Pin Name	LQFP-48 Pin No.	QFN-32 Pin No.	Type	Description
I2S_0_SCLK / DSD_0_SCLK_IN	48		I	***I2S serial clock input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial clock input:*** 3.3V TTL input, refer to DSD Specification.
I2S_0_SDATA / DSD_0_RIGHT_SDATA_IN	1		I	***I2S serial data input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial right data input:*** 3.3V TTL input, refer to DSD Specification.
I2S_0_SLR / DSD_0_LEFT_SDATA_IN	2		I	***I2S left/right input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial left data input:*** 3.3V TTL input, refer to DSD Specification.
I2S_1_SCLK / DSD_1_SCLK_IN	3	32	I	***I2S serial clock input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial clock input:*** 3.3V TTL input, refer to DSD Specification.
I2S_1_SDATA / DSD_1_RIGHT_SDATA_IN	4	1	I	***I2S serial data input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial right data input:*** 3.3V TTL input, refer to DSD Specification.
I2S_1_SLR / DSD_1_LEFT_SDATA_IN	5	2	I	***I2S left/right input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial left data input:*** 3.3V TTL input, refer to DSD Specification.
GND	6		G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
DVDD_12_CORE	7	3	P	***1.2V Core Power Connection:*** Power supply for all digital and MPLL function. Connect to 1.2V.
DVSS_12_CORE	8	4	G	***Ground Connection:*** Ground pins for all digital and MPLL function.
DVSS_PAD_0	9	5	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
DVDD_33_PAD_0	10	6	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
XTAL_IN	11	7	I	***External Crystal input:*** Connect to external crystal pin. Or external clock input. Selection : 12 / 11.2896 / 12.288 / 14.318 MHz
XTAL_OUT	12	8	O	***External Crystal output:*** Connect to external crystal pin
CLK_REF_OUT / POR_IN_6#	13	9	I/O	***Reference clock output:*** Crystal or internal PLL post clock output. ***Power on latch selection pin 6:*** I2C device ID selection [1]. Internal pull low 120 k-ohms.
I2S_2_SCLK / DSD_2_SCLK_IN	14		I	***I2S serial clock input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial clock input:*** 3.3V TTL input, refer to DSD Specification.
I2S_2_SDATA / DSD_2_RIGHT_SDATA_IN	15		I	***I2S serial data input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial right data input:*** 3.3V TTL input, refer to DSD Specification.
I2S_2_SLR / DSD_2_LEFT_SDATA_IN	16		I	***I2S left/right input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial left data input:*** 3.3V TTL input, refer to DSD Specification.
I2C_SCLK*	17	10	I	***I2C serial clock :*** Clock pin for serial interface. Refer to I2C specification. Internal pull high 120k-ohm.

Pin Name	LQFP-48 Pin No.	QFN-32 Pin No.	Type	Description
I2C_SDATA*	18	11	I/O	***I2C serial data :*** Data pin for serial interface. Refer to I2C specification. Internal pull high 120k-ohm.
INTERRUPT_Z*	19		O	***Interrupt open drain output:*** Internal pull high 120k-ohm.
DVDD_33_PAD_1	20	12	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_1	21	13	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
DSD_0_LEFT_SDATA_OUT / I2S_0_SLR_OUT POR_IN_5#	22	14	I/O	***DSD left serial data output:*** 3.3V TTL output, refer to DSD/ I2S Specification. ***Power on latch selection pin 5:*** I2C device ID selection [0]. Internal pull low 120k-ohm..
DSD_0_RIGHT_SDATA_OUT / I2S_0_SDATA_OUT POR_IN_4#	23	15	I/O	***DSD right serial data output:*** 3.3V TTL output, refer to DSD/ I2S Specification. ***Power on latch selection pin 4:*** Crystal frequency selection [1] Internal pull low 120k-ohm..
DSD_0_SCLK_OUT / I2S_0_SCLK_OUT POR_IN_3#	24	16	I/O	***DSD serial clock output:*** 3.3V TTL output, refer to DSD/ I2S Specification. ***Power on latch selection pin 3:*** Crystal frequency selection [0]. Internal pull low 120k-ohm..
DSD_MODE_OUT / POR_IN_2#	25		I/O	***DSD/DoP mode active status output:*** 3.3V TTL output, high active. ***Power on latch selection pin 2:*** reserved. Internal pull low 120k-ohm.
GND	26		G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
GND	27		G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
AVSS_12_LPLL	28	17	G	***Ground Connection:*** Ground pins for all LPLL function.
AVDD_12_LPLL	29	18	P	***1.2V Core Power Connection:*** Power supply for all PLL function. Connect to 1.2V.
GND	30		G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
I2S_1_SLR_OUT / DSD_1_LEFT_SDATA_OUT	31	19	I/O	***I2S left/right output:*** 3.3V TTL output, refer to DSD/ I2S Specification. Pin [31], [32], [33] support I2S Master/Slave mode.
I2S_1_SDATA_OUT / DSD_1_RIGHT_SDATA_OUT / POR_IN_1#	32	20	I/O	***I2S serial data output:*** 3.3V TTL output, refer to DSD/ I2S Specification. ***Power on latch selection pin 1:*** i2s tx slave mode selection. Pin [31], [32], [33] support I2S Master/Slave mode. Internal pull low 120 k-ohms.
I2S_1_SCLK_OUT / DSD_1_SCLK_OUT	33	21	I/O	***I2S serial clock output:*** 3.3V TTL output, refer to DSD/ I2S Specification. Pin [31], [32], [33] support I2S Master/Slave mode.
DVDD_33_PAD_2	34	22	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_2	35	23	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
I2S_MCLK_OUT / POR_IN_0#	36	24	I/O	***I2S master clock output:*** 3.3V TTL output, refer to DAC Document. ***Power on latch selection pin 0:*** reserved. Internal pull low 120 k-ohms.

Pin Name	LQFP-48 Pin No.	QFN-32 Pin No.	Type	Description
STATUS_SIGNAL_OUT	37		I/O	***Status mute signal output:*** 3.3V TTL output, refer to DAC Document. ***Power on latch***
ASRC_REF_CLK_IN#	38	25	I	***ASRC output clock reference input:*** 3.3V TTL input, refer to SRC selection table. Internal pull low 120 k-ohms.
SPDIF_OUT	39	26	O	***SPDIF output:*** 3.3V TTL output, refer to SPDIF Specification.
DVDD_33_PAD_3	40	27	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_3	41	28	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
SPDIF_0_IN	42	29	I	***SPDIF input channel 0:*** 200mV ~ 3.3 V single-end input, refer to SPDIF Specification.
SPDIF_1_IN	43	30	I	***SPDIF input channel 1:*** 200mV ~ 3.3 V single-end input, refer to SPDIF Specification.
SPDIF_2_IN	44 (NC.5302)		I	***SPDIF input channel 2:*** 200mV ~ 3.3 V single-end input. Refer to SPDIF Specification.
SPDIF_3_IN	45 (NC.5302)		I	***SPDIF input channel 3:*** 200mV ~ 3.3 V single-end input. Refer to SPDIF Specification.
SPDIF_4P_IN	46 (NC.5302)		I	***SPDIF input channel 4P:*** 200mV ~ 3.3 V differential input, refer to SPDIF Specification.
SPDIF_4N_IN / VREF	47	31	I	***SPDIF input channel 4N:*** 200mV ~ 3.3 V differential input, refer to SPDIF Specification ***SPDIF input Vref :*** internal SPDIF Vref. While CR1A.6 = 1.
I2S_0_SCLK / DSD_0_SCLK_IN	48		I	***I2S serial clock input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial clock input:*** 3.3V TTL input, refer to DSD Specification.

*Note: Internal 120K *pull-up or #pull down resistors present on inputs marked with *# respectively. Design should not rely solely on internal pull-up or pull down resistor to set I/O pins high or low respectively.*

LQFP 32 Pin Description

Pin Name	Pin No.	Type	Description
I2S_1_SCLK / DSD_1_SCLK_IN	32	I	***I2S serial clock input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial clock input:*** 3.3V TTL input, refer to DSD Specification.
I2S_1_SDATA / DSD_1_RIGHT_SDATA_IN	1	I	***I2S serial data input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial right data input:*** 3.3V TTL input, refer to DSD Specification.
I2S_1_SLR / DSD_1_LEFT_SDATA_IN	2	I	***I2S left/right input channel 2:*** 3.3V TTL input, refer to I2S Specification. ***DSD serial left data input:*** 3.3V TTL input, refer to DSD Specification.
DVDD_12_CORE	3	P	***1.2V Core Power Connection:*** Power supply for all digital and MPLL function. Connect to 1.2V.
DVSS_12_CORE	4	G	***Ground Connection:*** Ground pins for all digital and MPLL function.
DVSS_PAD_0	5	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
DVDD_33_PAD_0	6	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
XTAL_IN	7	I	***External Crystal input:*** Connect to external crystal pin. Or external clock input. Selection : 12 / 11.2896 / 12.288 / 14.318 MHz
XTAL_OUT	8	O	***External Crystal output:*** Connect to external crystal pin
CLK_REF_OUT / POR_IN_6#	9	I/O	***Reference clock output:*** Crystal or internal PLL post clock output. ***Power on latch selection pin 6:*** I2C device ID selection [1]. Internal pull low 120 k-ohms.
I2C_SCLK*	10	I	***I2C serial clock :*** Clock pin for serial interface. Refer to I2C specification. Internal pull high 120k-ohm.
I2C_SDATA*	11	I/O	***I2C serial data :*** Data pin for serial interface. Refer to I2C specification. Internal pull high 120k-ohm.
DVDD_33_PAD_1	12	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_1	13	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
DSD_0_LEFT_SDATA_OUT / I2S_0_SLR_OUT POR_IN_5#	14	I/O	***DSD left serial data output:*** 3.3V TTL output, refer to DSD/ I2S Specification. ***Power on latch selection pin 5:*** I2C device ID selection [0]. Internal pull low 120k-ohm..
DSD_0_RIGHT_SDATA_OUT / I2S_0_SDATA_OUT POR_IN_4#	15	I/O	***DSD right serial data output:*** 3.3V TTL output, refer to DSD/ I2S Specification. ***Power on latch selection pin 4:*** Crystal frequency selection [1] Internal pull low 120k-ohm..
DSD_0_SCLK_OUT / I2S_0_SCLK_OUT POR_IN_3#	16	I/O	***DSD serial clock output:*** 3.3V TTL output, refer to DSD/ I2S Specification. ***Power on latch selection pin 3:*** Crystal frequency selection [0]. Internal pull low 120k-ohm..
AVSS_12_LPLL	17	G	***Ground Connection:*** Ground pins for all LPLL function.
AVDD_12_LPLL	18	P	***1.2V Core Power Connection:*** Power supply for all PLL function. Connect to 1.2V.

Pin Name	Pin No.	Type	Description
I2S_1_SLR_OUT / DSD_1_LEFT_SDATA_OUT	19	I/O	***I2S left/right output:*** 3.3V TTL output, refer to DSD/ I2S Specification. Pin [19], [20], [21] support I2S Master/Slave mode.
I2S_1_SDATA_OUT / DSD_1_RIGHT_SDATA_OUT / POR_IN_1#	20	I/O	***I2S serial data output:*** 3.3V TTL output, refer to DSD/ I2S Specification. ***Power on latch selection pin 1:*** i2s tx slave mode selection. Pin [19], [20], [21] support I2S Master/Slave mode. Internal pull low 120 k-ohms.
I2S_1_SCLK_OUT / DSD_1_SCLK_OUT	21	I/O	***I2S serial clock output:*** 3.3V TTL output, refer to DSD/ I2S Specification. Pin [19], [20], [21] support I2S Master/Slave mode.
DVDD_33_PAD_2	22	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_2	23	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
I2S_MCLK_OUT / POR_IN_0#	24	I/O	***I2S master clock output:*** 3.3V TTL output, refer to DAC Document. ***Power on latch selection pin 0:*** reserved. Internal pull low 120 k-ohms.
ASRC_REF_CLK_IN#	25	I	***ASRC output clock reference input:*** 3.3V TTL input, refer to SRC selection table. Internal pull low 120 k-ohms.
SPDIF_OUT	26	O	***SPDIF output:*** 3.3V TTL output, refer to SPDIF Specification.
DVDD_33_PAD_3	27	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_3	28	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
SPDIF_0_IN	29	I	***SPDIF input channel 0:*** 200mV ~ 3.3 V single-end input, refer to SPDIF Specification.
SPDIF_1_IN	30	I	***SPDIF input channel 1:*** 200mV ~ 3.3 V single-end input, refer to SPDIF Specification.
VREF	31	I	***SPDIF input Vref :*** internal SPDIF Vref. While CR1A.6 = 1.

*Note: Internal 120K *pull-up or #pull down resistors present on inputs marked with *# respectively. Design should not rely solely on internal pull-up or pull down resistor to set I/O pins high or low respectively.*

Power on latch look up table

Pin Name	Description	Function Table
POR_IN_6 POR_IN_5	POWER_ON_LATCH_DC[6:5] = I2C_ID[1:0]	I2C serial interface device ID selection 00 = 0x20 01 = 0x22 10 = 0x24 11 = 0x26
POR_IN_4 POR_IN_3	POWER_ON_LATCH_DC[4:3] = SEL_XTAL[1:0]	Select Crystal frequency 00 = 12MHz 01 = 11.2896MHz 10 = 12.288MHz 11 = 14.318MHz
POR_IN_2	POWER_ON_LATCH_DC[2] = Reserved	Reserved
POR_IN_1	POWER_ON_LATCH_DC[1] = SEL_I2S_TX_SLAVE_MODE	Select I2S Tx Slave / Master mode 0 = master 1 = slave Pin [31], [32], [33] support I2S Master/Slave mode.
POR_IN_0	POWER_ON_LATCH_DC[0] = Reserved	Reserved

SRC software mode table

SRC Mode	Description	Output Frequency		
		Freq. Index Reg05[3:0]	Ratio Reg05[6:4]	Frequency
000	Synchronous to REFC_IN Fs input	-	-	Same as REFC_IN input clock
001	Synchronous to REFC_IN Fs input with ratio selector Fs output = Fs_{base} * N	-	000	1x Fs_{base} (32 / 44.1 / 48)
		-	001	2x Fs_{base} (64 / 88.2 / 96)
		-	010	4x Fs_{base} (128 / 176.4 / 192)
		-	011	8x Fs_{base} (256 / 352.8 / 384)
		-	100	16x Fs_{base} (512 / 705.6 / 768)
		-	others	reserve
010	Synchronous to REFC_IN MCLK input with ratio selector Fs output = Fs_{base} * N	-	000	1x Fs_{base} (32 / 44.1 / 48)
		-	001	2x Fs_{base} (64 / 88.2 / 96)
		-	010	4x Fs_{base} (128 / 176.4 / 192)
		-	011	8x Fs_{base} (256 / 352.8 / 384)
		-	100	16x Fs_{base} (512 / 705.6 / 768)
		-	others	reserve
011	Asynchronous, direct select target output frequency from index table Fs output = LUT(n)	0000	-	32 kHz
		0001	-	32 kHz
		0010	-	44.1KHz
		0011	-	48KHz
		0100	-	64 kHz
		0101	-	88.2 kHz
		0110	-	96 kHz
		0111	-	128 kHz
		1000	-	176.4 kHz
		1001	-	192 kHz
		1010	-	256 kHz
		1011	-	352.8 kHz
		1100	-	384 kHz
		1101	-	512 kHz
		1110	-	705.6 kHz
		1111	-	768 kHz

SRC Mode	Description	Output Frequency		
		Freq. Index Reg05[3:0]	Ratio Reg05[6:4]	Frequency
100	Synchronous to input port, direct select target output frequency from index table Fs output = LUT(n)	0000	-	32 kHz
		0001	-	32 kHz
		0010	-	44.1KHz
		0011	-	48KHz
		0100	-	64 kHz
		0101	-	88.2 kHz
		0110	-	96 kHz
		0111	-	128 kHz
		1000	-	176.4 kHz
		1001	-	192 kHz
		1010	-	256 kHz
		1011	-	352.8 kHz
		1100	-	384 kHz
		1101	-	512 kHz
		1110	-	705.6 kHz
		1111	-	768 kHz
101	synchronous to input with ratio selector Fs output = Fs_{base} * N	-	000	1x Fs_{base} (32 / 44.1 / 48)
		-	001	2x Fs_{base} (64 / 88.2 / 96)
		-	010	4x Fs_{base} (128 / 176.4 / 192)
		-	011	8x Fs_{base} (256 / 352.8 / 384)
		-	100	16x Fs_{base} (512 / 705.6 / 768)
		-	others	Reserve
110	BYPASS SRC	-		Fs output = Fs input
111	BYPASS SRC	-		Fs output = Fs input

Fix auto DSD + DoP output limitation table

DSD/DoP input	DSD output	DoP output
1x = 64xFs	1x = 64xFs	1x = PCM(4xFs)
2x = 128xFs	2x = 128xFs	2x = PCM(8xFs)
4x = 256xFs	4x = 256xFs	4x = PCM(16xFs)

*Fs = base sampling rate, means [32kHz or 44.1kHz or 48kHz]

*CR10.[6] = [0]

*CR4D.[0] = [0]

*CR59.[0] = [0]

Fix auto DSD + PCM output limitation table

DSD/DoP input	DSD output	PCM output
1x = 64xFs	1x = 64xFs	1xFs = [32,44,48] KHz
2x = 128xFs	2x = 128xFs	2xFs = [64,88,96] KHz
4x = 256xFs	4x = 256xFs	4xFs = [128,174,192] KHz
8xFs = 512xFs (DoP not suppout)	8xFs = 512xFs	8xFs = [256,352,384] KHz

*Fs = base sampling rate, means [32kHz or 44.1kHz or 48kHz]

*CR10.[6] = [1]

*CR4C.[3] = [0]

*CR4D.[0] = [0]

*CR59.[0] = [0]

Fix manual DSD + PCM output limitation table

DSD/DoP input	DSD output	PCM output
1x = 64xFs	Mute	1xFs = [32,44,48] KHz
2x = 128xFs		2xFs = [64,88,96] KHz
4x = 256xFs		4xFs = [128,174,192] KHz
8xFs = 512xFs		8xFs = [256,352,384] KHz
(DoP not suppout)		16xFs = [512,705,768] KHz

*Fs = base sampling rate, means [32kHz or 44.1kHz or 48kHz]

*CR10.[6] = [1]

*CR4C.[3] = [1]

*CR4C.[2:0] = select PCM output ratio.

*CR4D.[0] = [0]

*CR59.[0] = [0]

Fix DSD + SRC PCM output limitation table

DSD/DoP input	DSD output	PCM output
1x = 64xFs	Mute	[32,44,48] KHz
2x = 128xFs		[64,88,96] KHz
4x = 256xFs		[128,174,192] KHz
8xFs = 512xFs		[256,352,384] KHz
(DoP not suppout)		[512,705,768] KHz

*Fs = base sampling rate, means [32kHz or 44.1kHz or 48kHz]

*CR10.[6] = [1]

*CR4D.[0] = [1]

*CR59.[0] = [0]

*CR05.[3:0] = select PCM output frequency.

SRC DSD + PCM output limitation table

PCM/DSD/DoP input	PCM output	DSD output
PCM 32kHz ~ 768kHz DSD 1x ~ 8x DoP 1x ~ 4x	1xFs = [32,44,48] KHz	1x = 64xFs
	2xFs = [64,88,96] KHz	1x = 64xFs 2x = 128xFs
	4xFs = [128,174,192] KHz	1x = 64xFs 2x = 128xFs 4x = 256xFs
	8xFs = [256,352,384] KHz	1x = 64xFs 2x = 128xFs 4x = 256xFs 8x = 512xFs
	16xFs = [512,705,768] KHz	1x = 64xFs 2x = 128xFs 4x = 256xFs 8x = 512xFs

*Fs = base sampling rate, means [32kHz or 44.1kHz or 48kHz]

*CR59.[1:0] = [01]

*CR05.[3:0] = select PCM output frequency.

*CR59.[3:2] = select DSD output frequency.

SRC DSD + DoP output limitation table

PCM/DSD/DoP input	DSD output	DoP output
PCM 32kHz ~ 768kHz	1x = 64xFs	1x = PCM(4xFs)
DSD 1x ~ 8x	2x = 128xFs	2x = PCM(8xFs)
DoP 1x ~ 4x	4x = 256xFs	4x = PCM(16xFs)

*Fs = base sampling rate, means [32kHz or 44.1kHz or 48kHz]

*CR59.[1:0] = [11]

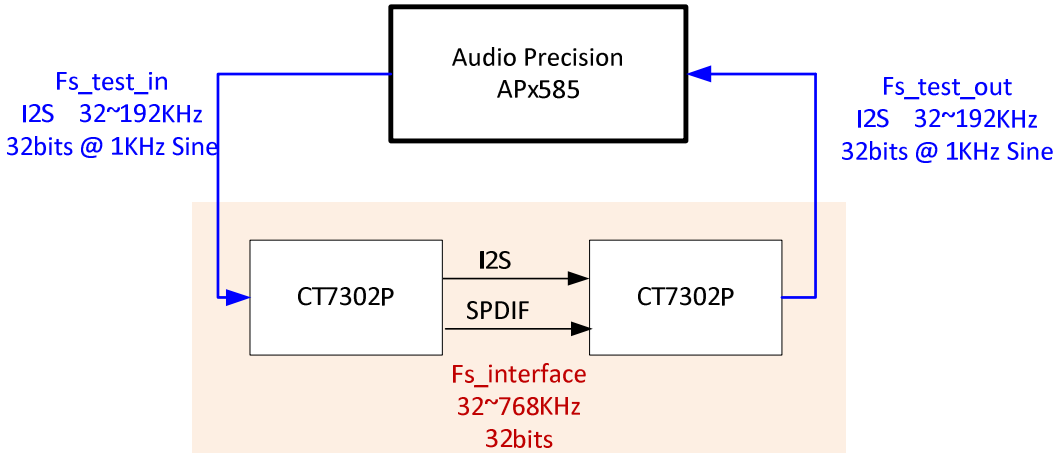
*CR59.[3:2] = select DSD/DoP output frequency.

DC specifications

Symbol	Parameter	Min.	Typical	Max.	Units	Notes
Absolute VDD CORE	1.2V core supply Voltage	-0.5	1.2	1.32	V	
Absolute VDD I/O	3.3V I/O supply Voltage	-0.5	3.3	3.6	V	
Ts	Storage Temperature	-65		150	ºC	
Ta	Ambient Temperature	0		70	ºC	
Absolute Vih	3.3V input high voltage	-0.5		3.6	V	
Absolute Vil	3.3V input low voltage	-0.5			V	
ESD	Input ESD protection	2			KV	Human body mode
Operating Vdd CORE	1.2V core supply Voltage	1.08	1.2	1.32	V	
Operating Vdd I/O	3.3V I/O supply Voltage	3.135	3.3	3.465	V	
Operating Vih	3.3V input high voltage	2.0		Vdd+0.3	V	
Operating Vil	3.3V input low voltage	Vss-0.3		0.8	V	
Operating Iil	Input leakage current	-5		+5	uA	
Operating Voh	3.3V output high voltage	2.4			V	Ioh=-1mA
Operating Vol	3.3V output low voltage			0.4	V	Iol=1mA
Cin	Input pin capacitance			5	pF	
Cxtal	XTAL pin capacitance	13.5		22.5	pF	17..20 pF
Cout	Output pin capacitance			6	pF	
Lpin	Pin inductance			7	nH	
I2S Setup time	3.3V I/O supply Voltage			7	nS	
I2S Hold time	3.3V I/O supply Voltage			100	pS	
Operating Current	3.3V active supply current		6	12	mA	
	1.2V active supply current		26	33	mA	
Power down	3.3V power down current	0.3			mA	
	1.2V power down current	0.2			mA	
SPDIF Rx Input Sensitivity,		0.100	0.200	3.300	V	

Sampling Rate Converter Characteristics

Test environment:



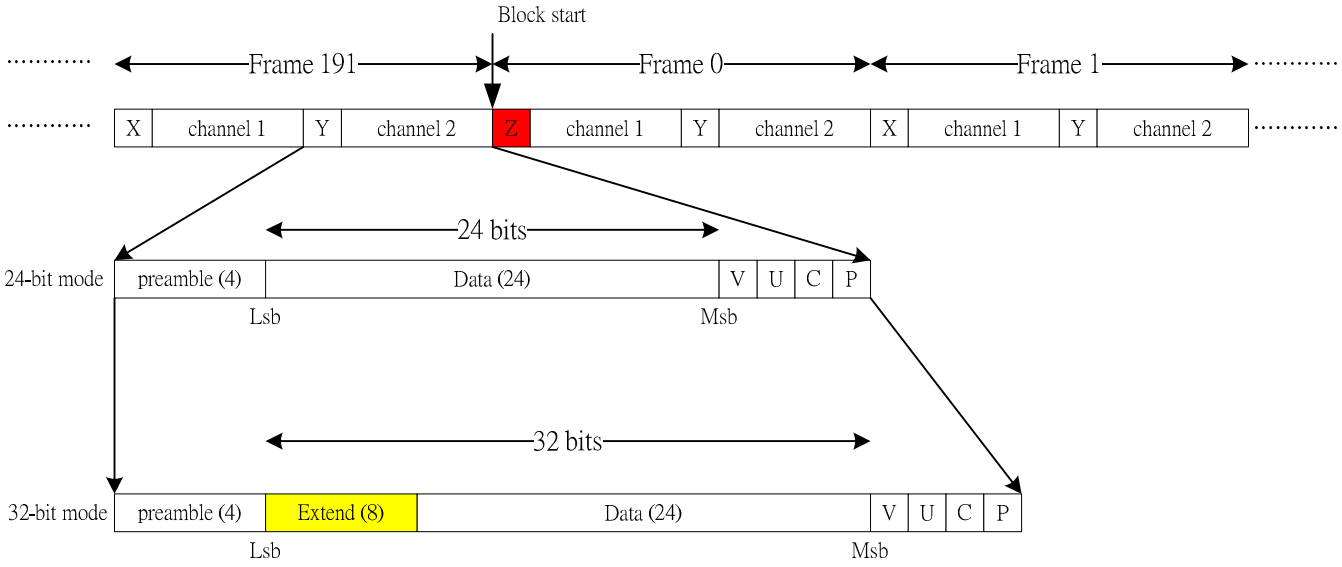
Test condition 32 bits input with audio precision (APx585) @1KHz, 0dB.

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Input Sampling Rate to test system: Fs_test_in	32 /44.1 /48 / 64/ 88.2/ 96/ 128/ 176.4/ 192	32		192	KHz
Interface Sampling Frequency: Fs_interface	32 /44.1 /48 / 64/ 88.2/ 96/ 128/ 176.4/ 192 256 /352.8 /384 / 512/ 705.6 /768	32		768	KHz
Output Sampling Rate from test system: Fs_test_out	32 /44.1 /48 / 64/ 88.2/ 96/ 128/ 176.4/ 192	32		192	KHz
Data path resolution			32		Bits
Dynamic Range (with A-weighting filter) Fs_test_in : Fs_interface : Fs_test_out = 32~192K : 32~768K : 32~192K any combination		190	191		dB
Total Harmonic Distortion + Noise (THD+N) (with A-weighting filter) Fs_test_in : Fs_interface : Fs_test_out = 32~192K : 32~768K : 32~192K any combination		-170	-174	-178	dB

Digital Filter Characteristics

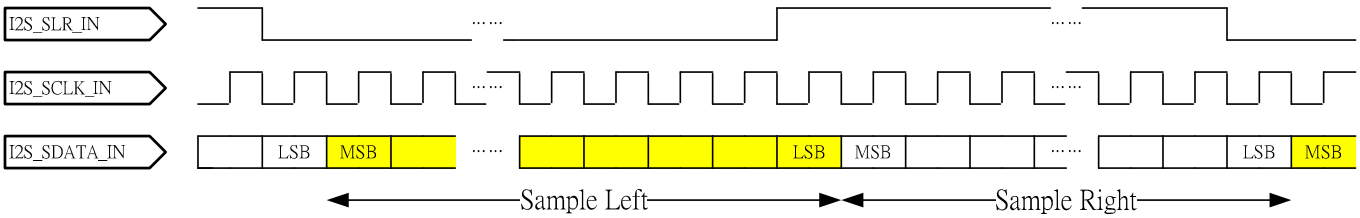
PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Interpolation Filter					
Passband				0.4535 x Fsin	Hz
Passband Ripple				±0.0001	dB
Stopband		0.5465 x Fsin			Hz
Stopband Attenuation		-144			dB
Group Delay				65.85/Fsin	Sec
Decimation Filter					
Passband				0.4535 x Fsin	Hz
Passband Ripple				±0.0001	dB
Stopband		0.5465 x Fsin			Hz
Stopband Attenuation		-144			dB
Group Delay				65.66/Fsin	Sec

SPDIF interface

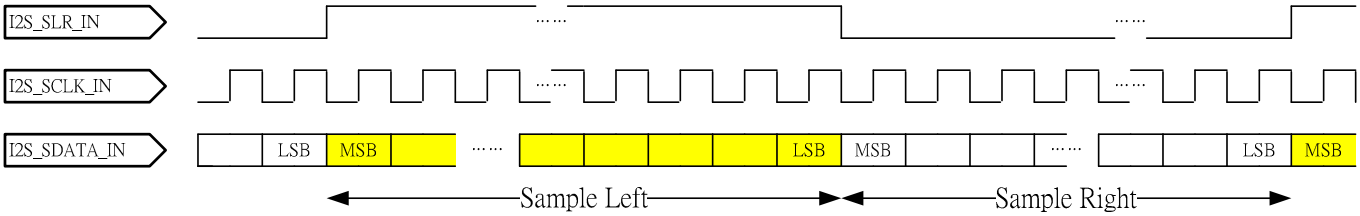


I2S interface

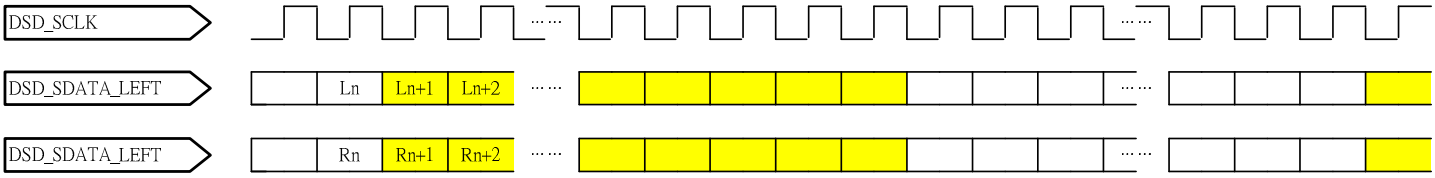
I2S standard format



I2S left justified format

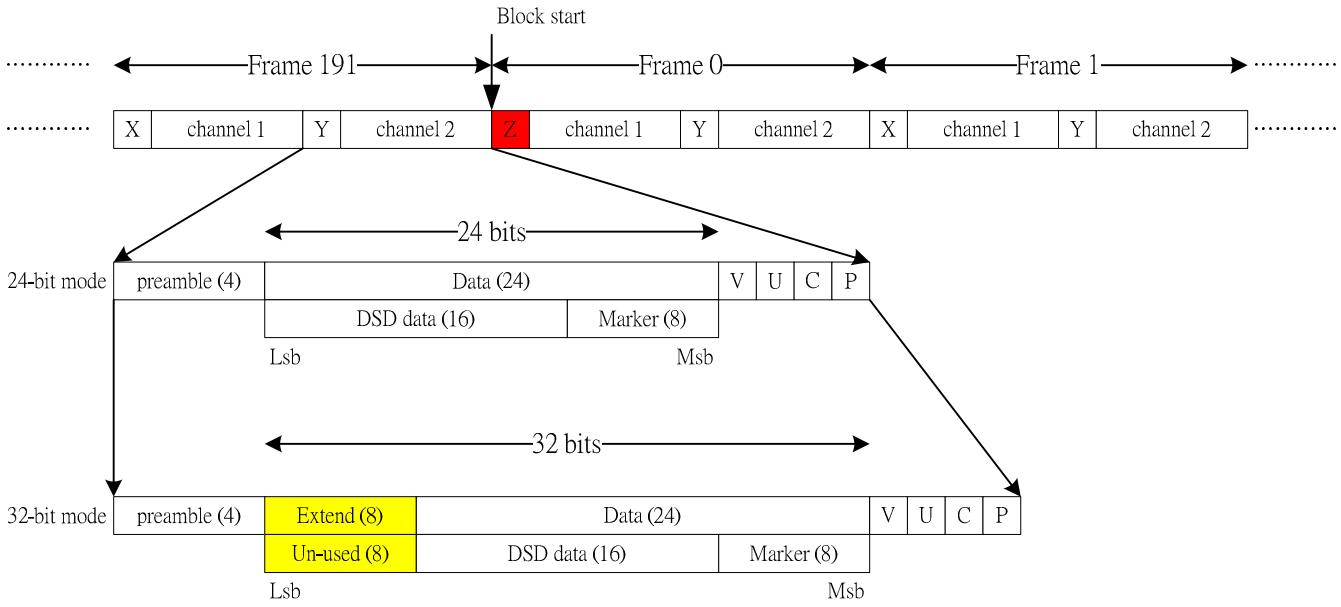


DSD interface



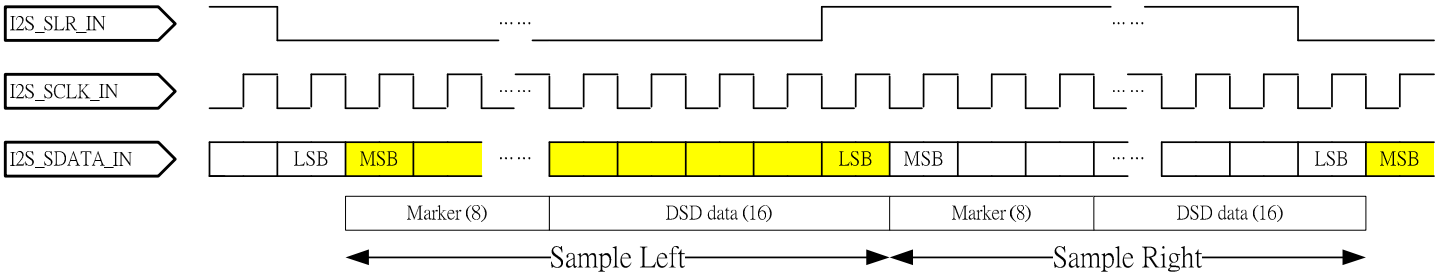
DoP interface

DSD over PCM through SPDIF

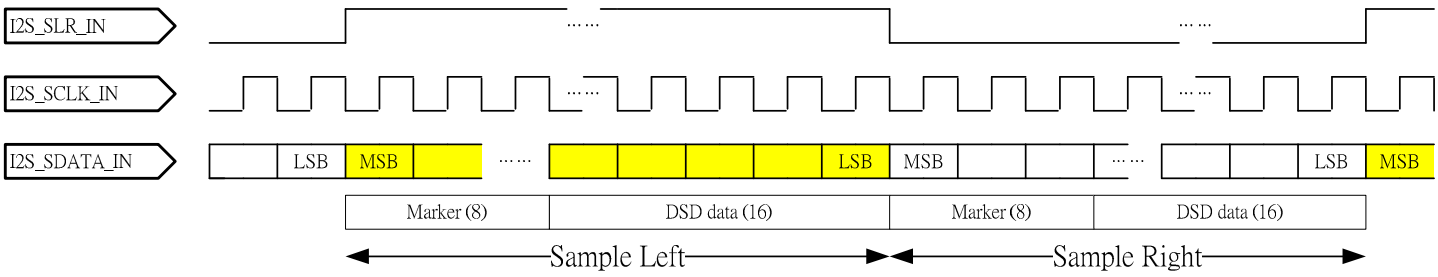


DSD over PCM through I2S

I2S standard format



I2S left justified format



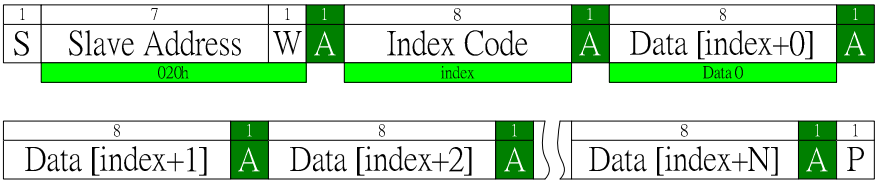
I2C interface

Register write command :

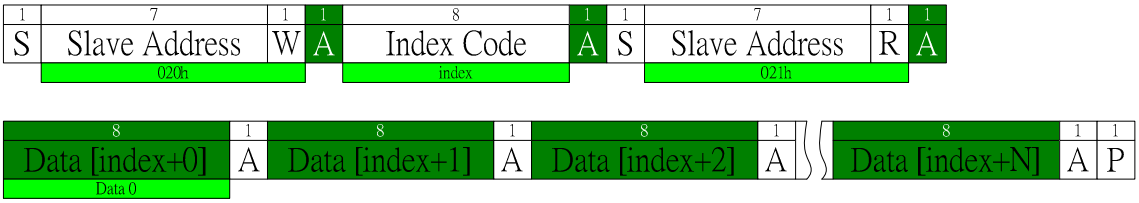
Slave address = 0x20

Register read command :

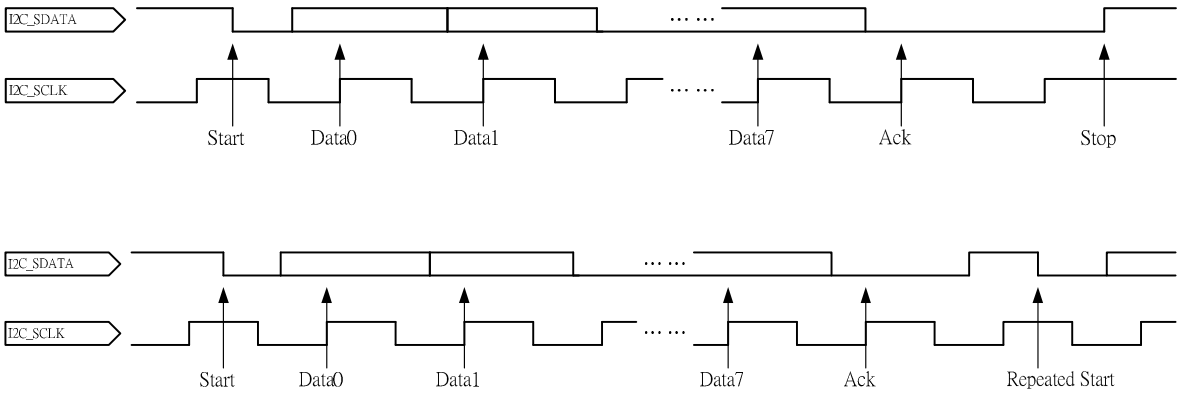
Slave address = 0x21



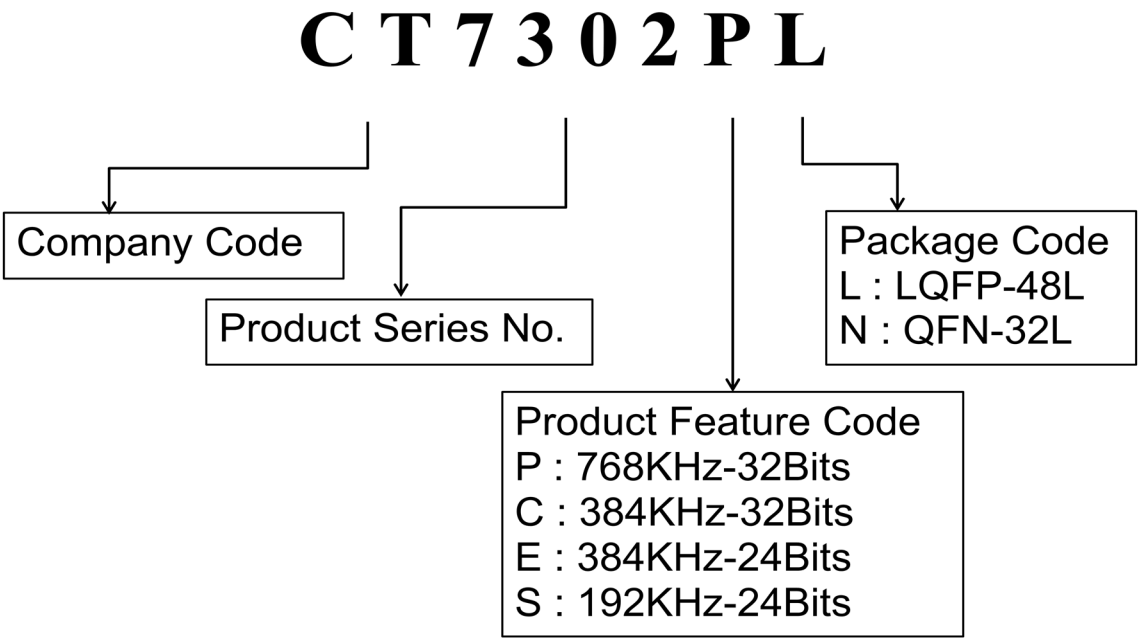
Block Write



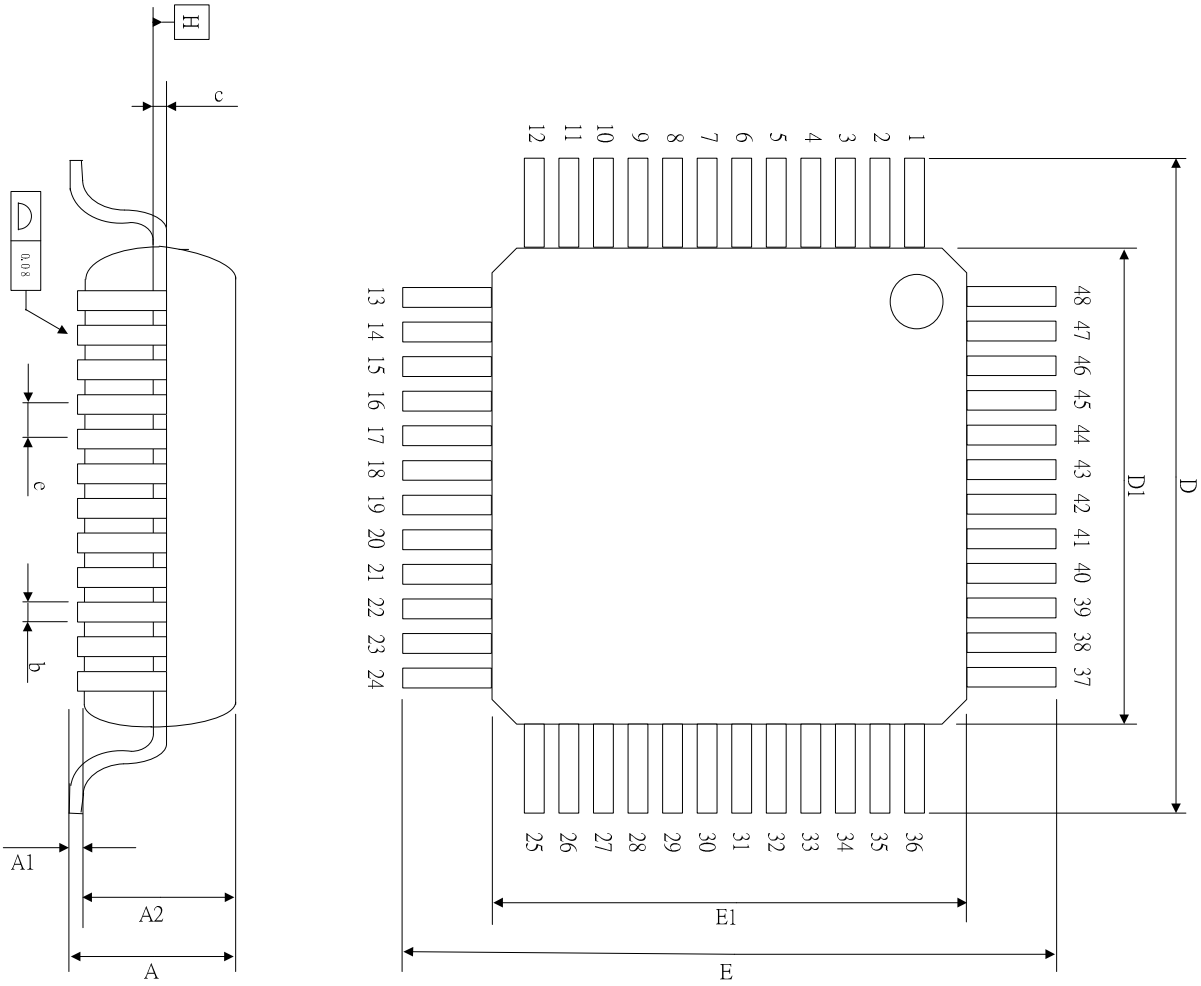
Block Read

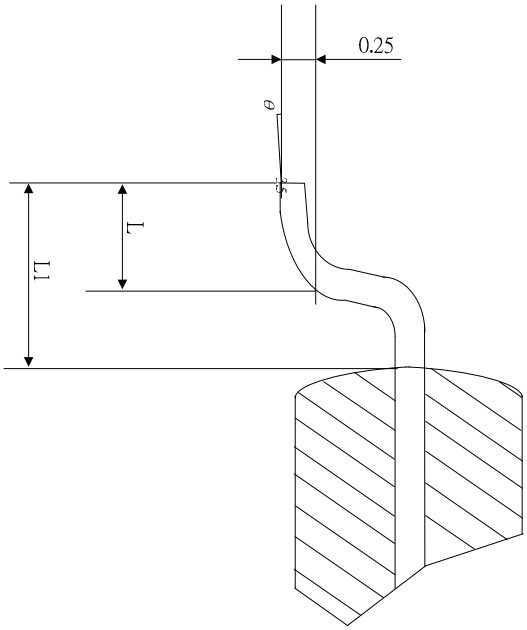


Naming rule



Package outline LQFP 48 pins



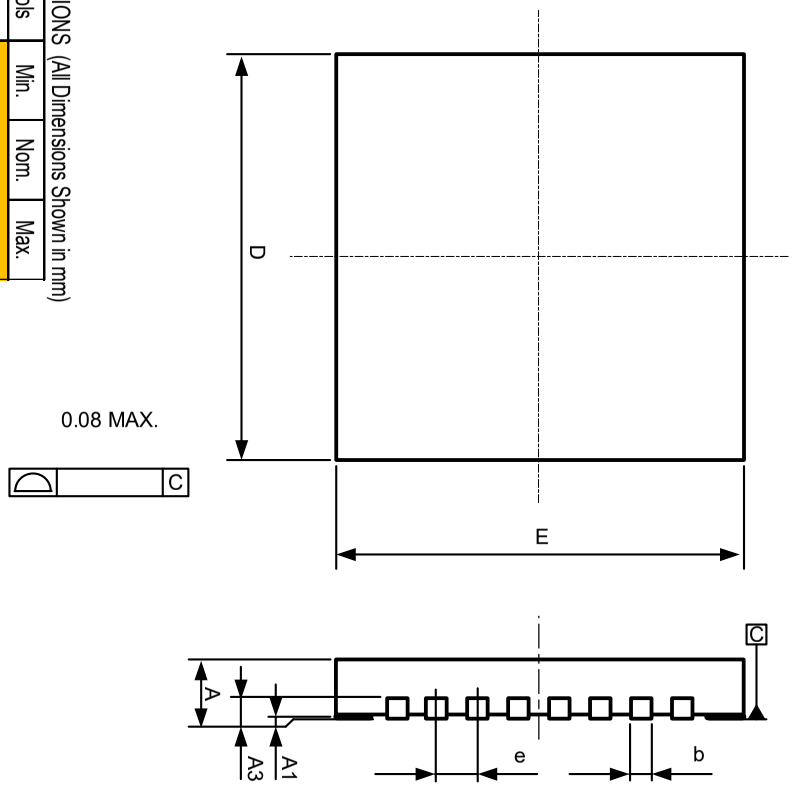


VARIATIONS (All Dimensions Shown in mm)			
Symbols	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	–	0.20
D		9.00 BSC	
D1		7.00 BSC	
E		9.00 BSC	
E1		7.00 BSC	
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

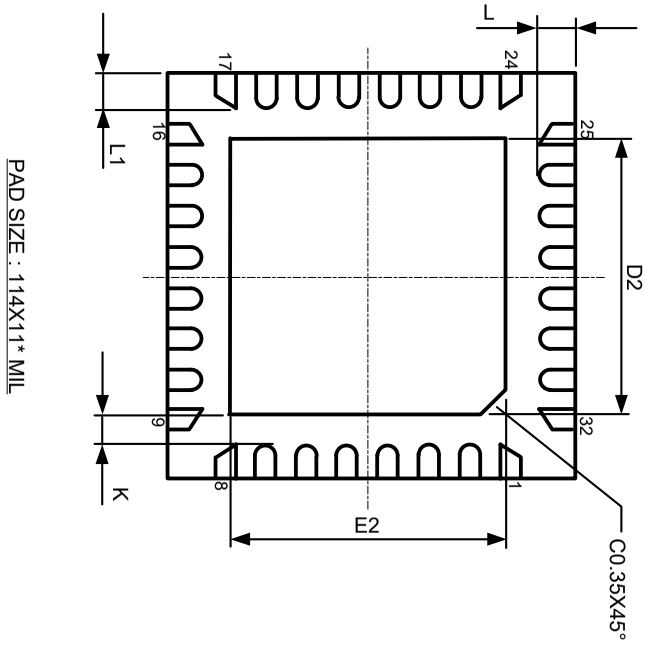
Package outline QFN 32 pins

VARIATIONS (All Dimensions Shown in mm)

Symbols	Min.	Nom.	Max.
PKG CODE		WQFN(X432)	
Symbols	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	



PAD SIZE	D2			E2			L			L1			K		
114X11*MIL	Min.	Nom.	Max.	Min.	Nom.	Max.	Min.	Nom.	Max.	Min.	Nom.	Max.	Min.	Nom.	Max.
	2.65	2.70	2.75	2.65	2.70	2.75	0.35	0.40	0.45	0.332	0.382	0.432	0.20	---	---



PAD SIZE : 114X11* MIL

0.85mm & 0.75mm : Leadframe 共用

Configuration register (I2C slave address = 0x20)

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
CONFIGURATION REGISTER						
0x00	REG_CFG_00 Default : [0x00]	RESERVED	7	R/W	0b	
		RESERVED	6	R/W	0b	
		RESERVED	5	R/W	0b	
		OUTPUT_PLL_IRQ	4	R/W	0b	Output pll IRQ (write 1 will clear this flag bit) 1 = IRQ 0 = normal Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
		INPUT_PLL_IRQ	3	R/W	0b	Input pll IRQ (write 1 will clear this flag bit) 1 = IRQ 0 = normal Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
		SPDIF_CDR_IRQ	2	R/W	0b	SPDIF clock data recovery IRQ (write 1 will clear this flag bit) 1 = IRQ 0 = normal Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
		KERNEL_IRQ	1	R/W	0b	Kernel IRQ (write 1 will clear this flag bit) 1 = IRQ 0 = normal Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
		SYSTEM_RESET_IRQ	0	R/W	0b	Power on reset IRQ (write 1 will clear this flag bit) 1 = IRQ 0 = normal Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
0x01	REG_CFG_01 Default : [0xfe]	RESERVED	7	R/W	1b	
		RESERVED	6	R/W	1b	
		RESERVED	5	R/W	1b	
		MASK_OUTPUT_PLL_IRQ	4	R/W	1b	Output pll IRQ mask 1 = mask 0 = normal Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
		MASK_INPUT_PLL_IRQ	3	R/W	1b	Input pll IRQ mask 1 = mask 0 = normal

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
		MASK_SPDIF_CDR_IRQ	2	R/W	1b	SPDIF clock data recovery IRQ mask 1 = mask 0 = normal Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
		MASK_KERNEL_IRQ	1	R/W	1b	Kernel IRQ mask 1 = mask 0 = normal Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
		MASK_SYSTEM_RESET_IRQ	0	R/W	0b	Power on reset IRQ mask 1 = mask 0 = normal Also refer to the reg.status.0x58 ~ 0x6E for interrupt service
0x02	REG_CFG_02 Default : [0x00]	KERNEL_IRQ_MASK mode_chg_124816_Q	7	R/W	0b	Mask mode_chg_124816_Q 1 = mask 0 = normal
		KERNEL_IRQ_MASK mode_chg_src_Q	6	R/W	0b	Mask mode_chg_src_Q 1 = mask 0 = normal
		KERNEL_IRQ_MASK mode_chg_dop_in_Q	5	R/W	0b	Mask mode_chg_dop_in_Q 1 = mask 0 = normal
		KERNEL_IRQ_MASK mode_chg_non_pcm_Q	4	R/W	0b	Mask mode_chg_non_pcm_Q 1 = mask 0 = normal
		KERNEL_IRQ_MASK in_pll_lock_in	3	R/W	0b	Mask in_pll_lock_in 1 = mask 0 = normal
		KERNEL_IRQ_MASK out_pll_lock_in	2	R/W	0b	Mask out_pll_lock_in 1 = mask 0 = normal
		KERNEL_IRQ_MASK in_pll_no_input	1	R/W	0b	Mask in_pll_no_input 1 = mask 0 = normal
		KERNEL_IRQ_MASK out_pll_no_input	0	R/W	0b	Mask out_pll_no_input 1 = mask

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						0 = normal
0x03	REG_CFG_03 Default : [0x00]	RESERVED	7	R/W	0b	
		RESERVED	6	R/W	0b	
		RESERVED	5	R/W	0b	
		KERNEL_IRQ_MASK cmp_mode_chg_de_emphasis_Q	4	R/W	0b	Mask cmp_mode_chg_de_emphasis_Q 1 = mask 0 = normal
		KERNEL_IRQ_MASK mode_chg_dop_to_pcm_Q	3	R/W	0b	Mask mode_chg_dop_to_pcm_Q 1 = mask 0 = normal
		KERNEL_IRQ_MASK mode_chg_spdif_rx_32_Q	2	R/W	0b	Mask mode_chg_spdif_rx_32_Q 1 = mask 0 = normal
		KERNEL_IRQ_MASK mode_chg_input_channel_Q	1	R/W	0b	Mask mode_chg_input_channel_Q 1 = mask 0 = normal
		KERNEL_IRQ_MASK mode_chg_freq_Q	0	R/W	0b	Mask mode_chg_freq_Q 1 = mask 0 = normal
0x04	REG_CFG_04 Default : [0x35]	RESERVED	7	R/W	0b	
		SW_SEL_SRC_MODE[2:0]	6:4	R/W	011b	Software sample rate convert mode selector 0 = asynchronous fs 1 = asynchronous fs + ratio_selector 2 = asynchronous 128fs + ratio_selector 3 = asynchronous + freq_selector 4 = synchronous to input + freq_selector 5 = synchronous to input + ratio_selector 6 = bypass SRC 7 = bypass SRC
		RESERVED	3	R/W	0b	
		SW_SEL_INPUT_CHANNEL[2:0]	2:0	R/W	101b	Software input channel selector 0 = SPDIF IN-0 1 = SPDIF IN-1 2 = SPDIF IN-2 3 = SPDIF IN-3 4 = SPDIF IN-4

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						5 = I2S IN-0 6 = I2S IN-1 7 = I2S IN-2 or DSD IN-0
0x05	REG_CFG_05 Default : [0x02]	~~SPDIF_OUT_PN_ACTIVE~~	~~7~~	~~R/W~~	~~0b~~	~~SPDIF differential output test mode~~ ~~0 = normal~~ ~~1 = test mode~~ ~~Only for internal test~~
		SW_SEL_SRC_RATIO_124816[2:0]	6:4	R/W	000b	Software SRC ratio selector 0 = 1x (32k/ 44k/ 48k) 1 = 2x (64k/ 88k/ 96k) 2 = 4x (128k/ 176k/ 192k) 3 = 8x (256k/ 352k/ 384k) 4 = 16x (512k/ 704k/ 768k) 5 = reserved 6 = reserved 7 = reserved
		SW_SEL_SRC_FREQUENCY[3:0]	3:0	R/W	0010b	Software SRC frequency selector 0 = 32 kHz 1 = 32 kHz 2 = 44.1 kHz 3 = 48 kHz 4 = 64 kHz 5 = 88.2 kHz 6 = 96 kHz 7 = 128 kHz 8 = 176.4 kHz 9 = 192 kHz A = 256 kHz B = 352.8 kHz C = 384 kHz D = 512 kHz E = 705.6 kHz F = 768 kHz
0x06	REG_CFG_06 Default : [0xc8]	FORCE_MUTE	7	R/W	1b	Mute control 0 = normal 1 = mute all output volume
		MUTE_PAD_INV	6	R/W	1b	Inverse STATUS pin from mute setting

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
						0 = mute signal 1 = inverse mute signal
		I2S_TX_FORMAT_SEL	5	R/W	0b	I2S Tx format setting 0 = STD format 1 = Left justified
		I2S_RX_FORMAT_SEL	4	R/W	0b	I2S Rx format setting 0 = STD format 1 = Left justified
		SET_I2S_TX_32_BIT	3	R/W	1b	I2S transmitter set to 32-bit data mode 0 = 24 bits 1 = 32 bits
		SET_SPDIF_TX_32_BIT	2	R/W	0b	SPDIF transmitter set to 32-bit data mode 0 = 24 bits 1 = 32 bits
		SOFT_WARE_DEPOP	1	R/W	0b	Software de-pop control 0 = auto de-pop 1 = force kernel engine into mute standby mode
		~~SET_SOFT_WARE_MODE~~	~~0~~	~~R/W~~	~~0b~~	~~Power on default is hardware mode~~ ~~0 = h/w mode~~ ~~1 = s/w mode~~
0x07	REG_CFG_07 Default : [0x03]	SET_I2S_TX_NON_PCM_AUTO_24_BIT	7	R/W	0b	Set I2S Tx auto change to 24-bit mode while non-pcm valid 0 = fix mode 1 = auto mode
		SET_SPDIF_TX_NON_PCM_AUTO_24_BIT	6	R/W	0b	Set SPDIF Tx auto change to 24-bit mode while non-pcm valid 0 = fix mode 1 = auto mode
		SET_I2S_TX_DOP_AUTO_24_BIT	5	R/W	0b	Set I2S Tx auto change to 24-bit mode while DoP valid 0 = fix mode 1 = auto mode
		SET_SPDIF_TX_DOP_AUTO_24_BIT	4	R/W	0b	Set SPDIF Tx auto change to 24-bit mode while DoP valid 0 = fix mode 1 = auto mode
		SET_VOLUME_DIRECT_BYPASS_MODE	3	R/W	0b	Volume control 0dB control mode while DoP or non-pcm 0 = gain setting 0dB 1 = bypass volume control

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
		SET_SPDIF_NON_PCM_MUTE_BYPASSZ	2	R/W	0b	SPDIF non-pcm output data setting 0 = pass non-pcm data 1 = mute data
		SET_AUTO_DE_EMPHASIS	1	R/W	1b	SPDIF input auto de-emphasis control 0 = disable auto function 1 = auto de-emphasis
		SET_RIGHT_VOLUME_EQ_LEFT	0	R/W	1b	Set volume control right channel equal to left channel 0 = independent 1 = equal
0x08	REG_CFG_08 Default : [0x00]	VOLUME_VALUE_RIGHT[3:0]	7:4	R/W	0000b	Volume control right channel [3:0]
		VOLUME_VALUE_LEFT[3:0]	3:0	R/W	0000b	Volume control left channel [3:0]
0x09	REG_CFG_09 Default : [0x24]	VOLUME_VALUE_LEFT [11:4]	7:0	R/W	24h	Volume control left channel [11:0] (step -0.03125dB) Offset P.dB = VOLUME_SHIFT_GAIN [1:0] 000h = 0 dB +P.dB 001h = -0.03125 dB +P.dB 240h = -18 dB +P.dB ….. FEF = -127.96875 dB +P.dB FFxh = mute
0x0A	REG_CFG_0A Default : [0x24]	VOLUME_VALUE_RIGHT [11:4]	7:0	R/W	24h	Volume control right channel [11:0] (step -0.03125dB) Offset P.dB = VOLUME_SHIFT_GAIN [1:0] 000h = 0 dB +P.dB 001h = -0.03125 dB +P.dB 240h = -18 dB +P.dB ….. FEF = -127.96875 dB +P.dB FFxh = mute If : SET_RIGHT_VOLUME_EQ_LEFT = 1 Then : VOLUME_VALUE_RIGHT = VOLUME_VALUE_LEFT
0x0B	REG_CFG_0B Default : [0x00]	SPDIF_TX_CH_STATUS[7:0]	7:0	R/W	00h	SPDIF Tx channel status[39:0] Refer to the IEC 60958-3
0x0C	REG_CFG_0C Default : [0x00]	SPDIF_TX_CH_STATUS[15:8]	7:0	R/W	00h	
0x0D	REG_CFG_0D	SPDIF_TX_CH_STATUS[23:16]	7:0	R/W	00h	

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
	Default : [0x00]					
0x0E	REG_CFG_0E Default : [0x31]	SPDIF_TX_CH_STATUS[31:24]	7:0	R/W	31h	
0x0F	REG_CFG_0F Default : [0x01]	SPDIF_TX_CH_STATUS[39:32]	7:0	R/W	01h	
0x10	REG_CFG_10 Default : [0xc0]	CLK_XTAL_OR_MPLL_12MHZ_SEL	7	R/W	1b	Reference clock output select 0 = SEL_CLK_REF_MANUAL[1:0], CR29h.[7:6] 1 = xtal clock SEL_CLK_REF_MANUAL[1:0] = CR29h.[7:6] : 00 = MPLL /24 = 12Mhz 01 = Xtal/2 10 = Xtal/4 11 = Xtal/8
		ENABLE_DOP_TO_PCM	6	R/W	1b	Set auto DoP to pcm convert 0 = DoP 1 = auto DoP to PCM convert
		FORCE_CMD_LATCH_ON	5	R/W	0b	Kernel mode change force latch without de-pop 0 = auto mode 1 = force latch mode change
		FORCE_STOP_REF_CLK	4	R/W	0b	Reference clock stop control 0 = enable clock output 1 = stop at 0
		FORCE_STOP_SPDIF_TX	3	R/W	0b	SPDIF Tx stop control 0 = enable clock output 1 = stop at 0
		FORCE_STOP_I2S_TX	2	R/W	0b	I2S_DSD_1 Tx stop control 0 = enable clock output 1 = stop at 0
		FORCE_STOP_DSD_TX	1	R/W	0b	I2S_DSD_0 Tx stop control 0 = enable clock output 1 = stop at 0
		FORCE_STOP_I2S_MCLK	0	R/W	0b	I2S mclk clock stop control 0 = enable clock output 1 = stop at 0
0x11	REG_CFG_11 Default : [0x03]	POWER_DOWN_ALL	7	R/W	0b	Power down all function 0 = normal

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
						1 = power down
		POWER_DOWN_XTAL	6	R/W	0b	Power down Xtal function 0 = normal 1 = power down
		POWER_DOWN_MPLL	5	R/W	0b	Power down mpll function 0 = normal 1 = power down
		POWER_DOWN_INPUT_LPLL	4	R/W	0b	Power down input pll function 0 = normal 1 = power down
		POWER_DOWN_OUTPUT_LPLL_0	3	R/W	0b	Power down output pll-0 : kernel / SPDIF function 0 = normal 1 = power down
		POWER_DOWN_OUTPUT_LPLL_1	2	R/W	0b	Power down output pll-1: I2S / DSD function 0 = normal 1 = power down
		FORCE_OSC_50MHZ_ON	1	R/W	1b	Force OSC 50Mhz free run 0 = normal 1 = free run
		FORCE_XTAL_FREE_RUN	0	R/W	1b	Force Xtal free run 0 = normal 1 = free run
0x12	REG_CFG_12 Default : [0x00]	SEL_SPDIF_TX_STOP_MODE	7	R/W	0b	Select stop behavior while enable mode change stopping Tx SPDIF output pin 0 = stop at low 1 = tri-state
		SEL_I2S_TX_STOP_MODE	6	R/W	0b	Select stop behavior while enable mode change stopping Tx I2S_DSD_1 output pin 0 = stop at low 1 = tri-state
		SEL_DSD_TX_STOP_MODE	5	R/W	0b	Select stop behavior while enable mode change stopping Tx I2S_DSD_0 output pin 0 = stop at low 1 = tri-state
		SEL_MCLK_STOP_MODE	4	R/W	0b	Select stop behavior while enable mode change stopping Tx MCLK output pin

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
						0 = stop at low 1 = tri-state
		ENABLE_MODE_CHG_PAD_STOP_SPDIF	3	R/W	0b	Enable mode change stop output pin function 0 = normal 1 = stop out
		ENABLE_MODE_CHG_PAD_STOP_I2S	2	R/W	0b	Enable mode change stop output pin function (I2S_DSD_1) 0 = normal 1 = stop out
		ENABLE_MODE_CHG_PAD_STOP_DSD	1	R/W	0b	Enable mode change stop output pin function (I2S_DSD_0) 0 = normal 1 = stop out
		ENABLE_MODE_CHG_PAD_STOP_MCLK	0	R/W	0b	Enable mode change stop output pin function 0 = normal 1 = stop out
0x13	REG_CFG_13 Default : [0xe0]	SPDIF_OUT_SEL_DE_JITTER	7	R/W	1b	SPDIF output pin de-jitter function 0 = normal 1 = de-jitter
		I2S_OUT_SEL_DE_JITTER	6	R/W	1b	I2S_DSD_1 output pin de-jitter function 0 = normal 1 = de-jitter
		DSD_OUT_SEL_DE_JITTER	5	R/W	1b	I2S_DSD_0 output pin de-jitter function 0 = normal 1 = de-jitter
		ALL_CLR_STATUS_TIMING_RE_SYNC	4	R/W	0b	All Timing generator re-sync signal status clear 0 = normal 0->1 = clear
		IN_SRC_CLR_STATUS_TIMING_RE_SYNC	3	R/W	0b	Input SRC Timing generator re-sync signal status clear 0 = normal 0->1 = clear
		OUT_SRC_CLR_STATUS_TIMING_RE_SYNC	2	R/W	0b	Output SRC Timing generator re-sync signal status clear 0 = normal 0->1 = clear
		I2S_TX_CLR_STATUS_TIMING_RE_SYNC	1	R/W	0b	I2S output Timing generator re-sync signal status clear 0 = normal 0->1 = clear
		DSD_TX_CLR_STATUS_TIMING_RE_SYNC	0	R/W	0b	DSD output Timing generator re-sync signal status clear

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						0 = normal 0->1 = clear
0x14	REG_CFG_14 Default : [0x52]	FORCE_BYPASS_VOLUME	7	R/W	0b	Bypass volume test mode control function 0 = normal 1 = bypass volume control, only for test
		SET_CHANNEL_STATUS_PASS_THROUGH	6	R/W	1b	SPDIF Tx channel status selection 0 = from register setting 1 = from SPDIF Rx if input channel select SPDIF-IN
		FADING_MODE[1:0]	5:4	R/W	01b	Volume control fading mode selection 00 = normal 01 = DC detector 10 = test mode fading in 11 = test mode fading out
		VOLUME_CMP_PERIOD[3:0]	3:0	R/W	0010b	Volume control DSP step N-sample Command period = N + 1 sample
0x15	REG_CFG_15 Default : [0xc0]	ZERO_CROSS_THRESHOLD[15:8]	7:0	R/W	C0h	Volume control DC detector non-zero-cross sample DC sample = { ZERO_CROSS_THRESHOLD[15:8],0xfc}
0x16	REG_CFG_16 Default : [0x56]	DSD_HOLD_REPLACE_DATA[7:0]	7:0	R/W	56h	DSD output mute signal pattern[7:0]
0x17	REG_CFG_17 Default : [0x06]	DOP_MARKER_EXT [7:0]	7:0	R/W	06h	DoP marker extend from FA/05 Default = F9/06
0x18	REG_CFG_18 Default : [0x05]	DSD_TO_DOP_MARKER [7:0]	7:0	R/W	05h	DSD to DoP or DoP replace marker Default = FA/05
0x19	REG_CFG_19 Default : [0x20]	DOP_DETECT_CNT[7:0]	7:0	R/W	20h	DoP detector marker counter If : marker sample > DOP_DETECT_CNT+1 Then : DoP_flag = 1
0x1A	REG_CFG_1A Default : [0x41]	DSD_RX_SAMPLE_LR_CHANGE	7	R/W	0b	DSD Rx sample left/right swap 0 = normal 1 = swap
		SPDIF_VCOM_MODE	6	R/W	1b	SPDIF input Vcom mode selection 0 = internal V-common mode (spdif-4 differential mode) 1 = external V-common mode (sdif-4 single-end mode)
		FORCE_DE_EMPHASIS	5	R/W	0b	Force de-emphasis filter active 0 = normal

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						1 = force active
		DOP_ALIGN_LR_EN	4	R/W	0b	DoP marker check rule setting 0 = normal 1 = alignment rule
		SET_DOP_MARKER_REPLACE	3	R/W	0b	DoP Tx marker replace with register 0 = from Rx 1 = from register DSD_TO_DOP_MARKER[7:0]
		DSD_TX_SAMPLE_LR_CHANGE	2	R/W	0b	DSD Tx sample left/right swap 0 = normal 1 = swap
		DOP_DISABLE_CNT[1:0]	1:0	R/W	01b	DoP detector marker counter If : Un-marker sample > DOP_DISABLE_CNT+1 Then : DoP_flag = 0
0x1B	REG_CFG_1B Default : [0xa7]	ZR_DE_EMPHASIS_TEST_MODE	7	R/W	1b	De_emphasis mode selector 0 = auto mute mode before de_emphasis 1 = direct de_emphasis mode
		SEL_CLK_528MHZ_SPDIF_CDR_SYNTHESIZER	6	R/W	0b	Select SPDIF CDR reference clock 0 = 576 MHz 1= 288 MHz
		SEL_CLK_125MHZ_FILTER_MAC_DSP_DAC[1:0]	5:4	R/W	10b	Up-sample filter MAC clock selection 00 = 288 MHz 01 = INPUT_LPLL_SRC_200MHZ_CLK * 10 = 192MHz 11 = 144 MHz
		SEL_CLK_125MHZ_FILTER_MAC_DSP_ADC[1:0]	3:2	R/W	01b	Down-sample filter MAC clock selection 00 = 144 MHz 01 = 115 MHz 10 = 96 MHz 11 = OUTPUT_I2S_LPLL_SRC_100MHZ_CLK*
		SEL_CLK_125MHZ_SRC_MAC_DSP[1:0]	1:0	R/W	11b	SRC filter MAC clock selection 00 = 115 MHz 01 = 96 MHz 10 = 82 MHz 11 = 72 MHz

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
0x1C	REG_CFG_1C Default : [0x02]	INV_CLK_50MHZ_I2S_RX_BCLK	7	R/W	0b	Inverse I2S Rx clock system 0 = normal 1 = inverse
		INV_CLK_25MHZ_DSD_RX_BCLK	6	R/W	0b	Inverse DSD Rx clock system 0 = normal 1 = inverse
		INV_CLK_125MHZ_OUTPUT_SYSTEM_128_160_FS	5	R/W	0b	Inverse output kernel clock system 0 = normal 1 = inverse
		INV_CLK_125MHZ_SPDIF_TX_128_160_FS	4	R/W	0b	Inverse SPDIF Tx clock system 0 = normal 1 = inverse
		INV_CLK_50MHZ_I2S_TX_BCLK_48_64_FS	3	R/W	0b	Inverse I2S Tx clock system 0 = normal 1 = inverse
		INV_CLK_25MHZ_DSD_TX_BCLK_16_4FS	2	R/W	0b	Inverse DSD Tx clock system 0 = normal 1 = inverse
		OUT_LPLL_1_SEL_MCLK[1:0]	1:0	R/W	10b	I2S MCLK output setting fs base = 32/44.1/48 KHz 00 = 6 MHz base (fs base *128) 01 = 12 MHz base (fs base *256) 10 = 24 MHz base (fs base *512) 11 = 48 MHz base (fs base *1024)
0x1D	REG_CFG_1D Default : [0x7b]	ENABLE_CLK_250MHZ_OSC_POST_SYNTHESIZER	7	R/W	0b	Force clock enable 0 = auto 1 = force on
		ENABLE_CLK_264MHZ_MPLL_FEEDBACK_SYNTHESIZER	6	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_264MHZ_MPLL_POST_SYNTHESIZER	5	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_264MHZ_INPUT_LPLL_SYNTHESIZER	4	R/W	1b	Enable clock system 0 = stop 1 = enable

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
		ENABLE_CLK_264MHZ_OUTPUT_LPLL_SYNTHESIZER	3	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_200MHZ_SRC_MF_RATIO_SYNTHESIZER	2	R/W	0b	Force clock enable 0 = auto 1 = force on
		ENABLE_CLK_132MHZ_SYNTHESIZER_REF_INPUT_SPDIF_I2S_DSD	1	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_132MHZ_SYNTHESIZER_REF_INPUT_SRC_8_MODE	0	R/W	1b	Enable clock system 0 = stop 1 = enable
0x1E	REG_CFG_1E Default : [0xcf]	ENABLE_CLK_125MHZ_INPUT_SYSTEM_128_FS	7	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_125MHZ_OUTPUT_SYSTEM_128_160_FS	6	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_125MHZ_FILTER_MAC_DSP	5	R/W	0b	Force clock enable 0 = auto 1 = force on
		ENABLE_CLK_125MHZ_SRC_MAC_DSP	4	R/W	0b	Force clock enable 0 = auto 1 = force on
		ENABLE_CLK_125MHZ_SPDIF_TX_128_160_FS	3	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_50MHZ_I2S_TX_BCLK_48_64_FS	2	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_25MHZ_DSD_TX_BCLK_16_4FS	1	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_1MHZ_TIMER	0	R/W	1b	Enable clock system 0 = stop 1 = enable

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
0x1F	REG_CFG_1F Default : [0x5e]	SEL_MPLL_264MHZ_SOURCE	7	R/W	0b	Mpll reference input clock manual mode 0 = OSC 50MHz 1 = Xtal
		SET_XTAL_AUTO_DETECT	6	R/W	1b	Mpll reference input clock auto detection 0 = select by SEL_MPLL_264MHZ_SOURCE 1 = select by xtal auto detector
		ENABLE_CLK_12MHZ_MPLL_DIV_22	5	R/W	0b	Force clock enable 0 = auto 1 = force on
		ENABLE_CLK_16KHZ_TIMER	4	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_50MHZ_IN_LPLL_0_REF_IN	3	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_50MHZ_OUT_LPLL_0_REF_IN	2	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_50MHZ_OUT_LPLL_1_REF_IN	1	R/W	1b	Enable clock system 0 = stop 1 = enable
		ENABLE_CLK_50MHZ_MPLL_FEEDBACK_IN	0	R/W	0b	Force clock enable 0 = auto 1 = force on
0x20	REG_CFG_20 Default : [0xf6]	MPLL_FEEDBACK_N_F_OSC_FREQ [7:0]	7:0	R/W	f6h	MPLL_FEEDBACK_N_F_OSC_FREQ [23:0] = 5.19 Mpll output clock = OSC_25* N.f = 288MHz
0x21	REG_CFG_21 Default : [0x28]	MPLL_FEEDBACK_N_F_OSC_FREQ [15:8]	7:0	R/W	28h	
0x22	REG_CFG_22 Default : [0x5c]	MPLL_FEEDBACK_N_F_OSC_FREQ [23:16]	7:0	R/W	5ch	
0x23	REG_CFG_23 Default : [0x00]	MPLL_FEEDBACK_N_F_PRG_FREQ [7:0]	7:0	R/W	00h	MPLL_FEEDBACK_N_F_PRG_FREQ[23:0]= 5.19 Mpll feedback clock = Mpll/ N.f = Xtal While MPLL_FEEDBACK_SEL_N_F_PRG_FREQ = 1
0x24	REG_CFG_24 Default : [0xc0]	MPLL_FEEDBACK_N_F_PRG_FREQ [15:8]	7:0	R/W	c0h	
0x25	REG_CFG_25 Default : [0x5d]	MPLL_FEEDBACK_N_F_PRG_FREQ [23:16]	7:0	R/W	5dh	

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
0x26	REG_CFG_26 Default : [0x73]	MPLL_POST_N_F_PRG_FREQ [7:0]	7:0	R/W	73h	MPLL_POST_N_F_PRG_FREQ [23:0]= 5.19 Mpll post clock = Mpll/ N.f = 512 * Fs-out Only for SRC mode-3 While MPLL_POST_SEL_N_F_PRG_FREQ = 1
0x27	REG_CFG_27 Default : [0x0a]	MPLL_POST_N_F_PRG_FREQ [15:8]	7:0	R/W	0ah	
0x28	REG_CFG_28 Default : [0x66]	MPLL_POST_N_F_PRG_FREQ [23:16]	7:0	R/W	66h	
0x29	REG_CFG_29 Default : [0x08]	SEL_CLK_REF_MANUAL[1:0]	7:6	R/W	00b	CLK_REF output selection while manual mode 00 = MPLL /24 = 12Mhz 01 = Xtal/2 10 = Xtal/4 11 = Xtal/8
		MPLL_FEEDBACK_SEL_N_F_PRG_FREQ	5	R/W	0b	Mpll feedback /N.f selection 0 = look up table 1 = register programming mode
		MPLL_POST_SEL_N_F_PRG_FREQ	4	R/W	0b	Mpll post /N.f selection 0 = look up table 1 = register programming mode
		OSC_50MHZ_FREQ_SEL[3:0]	3:0	R/W	1000b	OSC frequency selection 0000 = min 1000 = mid 50MHz 1111 = max
0x2A	REG_CFG_2A Default : [0x96]	MPLL_SEL_EXT_IN	7	R/W	1b	Mpll feedback clock selection 0 = fix divider N 1 = divider N.f
		MPLL_SEL_FEEDBACK_DIV[6:0]	6:0	R/W	001-0110b	Mpll fix divider N N = MPLL_SEL_FEEDBACK_DIV[6:0] + 2
0x2B	REG_CFG_2B Default : [0x00]	IN_LPLL_RESET	7	R/W	0b	Input LPLL reset Vc 0 = normal 1 = reset Vc
		IN_LPLL_SEL_IB[2:0]	6:4	R/W	000b	Input pll bias current selection 0 = min 1 = …. 7 = max
		MPLL_RESET	3	R/W	0b	Mpll reset Vc 0 = normal

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
						1 = reset Vc
		MPLL_SEL_IB[2:0]	2:0	R/W	000b	Mpll bias current selection 0 = min 1 = …. 7 = max
0x2C	REG_CFG_2C Default : [0x00]	OUT_LPLL_1_RESET	7	R/W	0b	Output LPLL-1 reset Vc 0 = normal 1 = reset Vc
		OUT_LPLL_1_SEL_IB[2:0]	6:4	R/W	000b	output pll-1 bias current selection 0 = min 1 = …. 7 = max
		OUT_LPLL_0_RESET	3	R/W	0b	Output LPLL-0 reset Vc 0 = normal 1 = reset Vc
		OUT_LPLL_0_SEL_IB[2:0]	2:0	R/W	000b	output pll-0 bias current selection 0 = min 1 = …. 7 = max
0x2D	REG_CFG_2D Default : [0x54]	CDR_LPF_CS_PRG_FREQ [7:0]	7:0	R/W	54h	CDR_LPF_CS_PRG_FREQ[20] = CDR_LPF_CS_PRG_FREQ_ext_msb CDR_LPF_CS_PRG_FREQ[20:0] = 8.13 SPDIF CDR CLOCK = 528MHz/ N.f
0x2E	REG_CFG_2E Default : [0x30]	CDR_LPF_CS_PRG_FREQ [15:8]	7:0	R/W	30h	
0x2F	REG_CFG_2F	CDR_LPF_CS_PRG_FREQ [19:16]	3:0	R/W	3h	
	Default : [0x73]	CDR_FREQ_GAIN_COARSE[3:0]	7:4	R/W	0111b	SPDIF CDR coarse frequency gain setting 0000 = min 1111 = max
0x30	REG_CFG_30 Default : [0x57]	CDR_FREQ_COARSE_1X_OFFSET_K[3:0]	7:4	R/W	0101b	SPDIF CDR frequency detector 1x offset setting 0 = min 1 = …. F = max
		CDR_FREQ_COARSE_3X_OFFSET_K[3:0]	3:0	R/W	0111b	SPDIF CDR frequency detector 3x offset setting

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						0 = min 1 = …. F = max
0x31	REG_CFG_31 Default : [0x08]	RESERVED	7	R/W	0b	
		CDR_PHASE_CS_GAIN_FINE[6:0]	6:0	R/W	08h	SPDIF CDR phase detector Cs fine gain setting 00h = min 3fh = max
0x32	REG_CFG_32 Default : [0x1e]	RESERVED	7	R/W	0b	
		CDR_PHASE_VC_GAIN_FINE[6:0]	6:0	R/W	1eh	SPDIF CDR phase detector Vc fine gain setting 00h = min 3fh = max
0x33	REG_CFG_33 Default : [0x0d]	ENABLE_CHK_SPDIF_BLOCK_LOCKED	7	R/W	0b	Kernel system check SPDIF Rx decoder block locked 0 = not check 1 = check block locked signal
		CDR_LOCK_IN_GLITCH_CLR_CTRL	6	R/W	0b	SPDIF CDR lock-in glitch clear setting 0 = normal 0->1 = clear IRQ
		CDR_LOCK_IN_IRQ_CLR_CTRL	5	R/W	0b	SPDIF CDR lock-in IRQ clear setting 0 = normal 0->1 = clear IRQ
		CDR_NO_INPUT_IRQ_CLR_CTRL	4	R/W	0b	SPDIF CDR no-input IRQ clear setting 0 = normal 0->1 = clear IRQ
		ENABLE_IRQ_CDR_LOCK_IN	3	R/W	1b	SPDIF CDR lock-in IRQ setting 0 = disable IRQ 1 = enable IRQ
		ENABLE_IRQ_CDR_NO_INPUT	2	R/W	1b	SPDIF CDR no-input IRQ setting 0 = disable IRQ 1 = enable IRQ
		ENABLE_CDR_NO_INPUT_AUTO_PRG	1	R/W	0b	SPDIF CDR no-input auto manual frequency setting 0 = normal 1 = no-input manual programming mode
		ENABLE_SPDIF_CDR	0	R/W	1b	SPDIF CDR enable control 0 = off 1 = on

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
0x34	REG_CFG_34 Default : [0xc1]	SPDIF_RX_ERROR_HOLD_OLD_SAMPLE	7	R/W	1b	SPDIF CDR decoder hold old sample if any error 0 = disable 1 = enable
		COMBINE_IN_PLL_NO_INPUT_STATUS	6	R/W	1b	SPDIF CDR no-input detector status transfer to next stage 0 = disable 1 = to next stage
		CDR_LOCK_FREQ_STATUS_READ	5	R/W	0b	SPDIF CDR frequency status read back 0 = read 1 time 1 = enable continue read back
		CDR_FREQ_PRG_MODE	4	R/W	0b	SPDIF CDR test mode 0 = normal 1 = manual programming mode
		CDR_FREQ_LOCK_CURRENT_MODE	3	R/W	0b	SPDIF CDR test mode 0 = normal 1 = lock frequency detector
		CDR_PHASE_LOCK_CURRENT_MODE	2	R/W	0b	SPDIF CDR test mode 0 = normal 1 = lock phase detector
		CDR_SKEW_CTRL[1:0]	1:0	R/W	01b	SPDIF CDR clock & data skew control 00 = clock early 1T 01 = sync 10 = delay 1T 11 = delay 2T
0x35	REG_CFG_35 Default : [0xa5]	PLL_DC_CMP_8X_4X_2X_1X[7:0]	7:0	R/W	a5h	Lpll frequency bank compare value
0x36	REG_CFG_36 Default : [0x8d]	PLL_FREQ_DC_CMP_32K[7:0]	7:0	R/W	8dh	Lpll frequency bank compare value
0x37	REG_CFG_37 Default : [0x66]	PLL_FREQ_DC_CMP_44K[7:0]	7:0	R/W	66h	Lpll frequency bank compare value
0x38	REG_CFG_38 Default : [0x5e]	PLL_FREQ_DC_CMP_48K[7:0]	7:0	R/W	5eh	Lpll frequency bank compare value
0x39	REG_CFG_39 Default : [0xa3]	OUT_PLL_SEL_X_FS_BAND_WIDTH[1:0]	7:6	R/W	10b	Output lpll charge pump frequency bandwidth setting 00 = 32 fs 01 = 64 fs 10 = 128 fs 11 = 256 fs

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
		IN_PLL_SEL_X_FS_BAND_WIDTH[1:0]	5:4	R/W	10b	Input lpll charge pump frequency bandwidth setting 00 = 32 fs 01 = 64 fs 10 = 128 fs 11 = 256 fs
		PLL_FREQ_DC_CMP_OFFSET[3:0]	3:0	R/W	0011b	Lpll frequency detector offset (32/44/48/64/88 …./768) 0000 = min 0011 = default 1111 = max
0x3A	REG_CFG_3A Default : [0x29]	PLL_DC_CMP_4X_205KHZ[7:0]	7:0	R/W	29h	Lpll frequency bank compare value
0x3B	REG_CFG_3B Default : [0x77]	OUT_PLL_FREQ_LOCK_IN_OFFSET_K[3:0]	7:4	R/W	0111b	Output lpll lock in compare value
		IN_PLL_FREQ_LOCK_IN_OFFSET_K[3:0]	3:0	R/W	0111b	Output lpll lock in compare value
0x3C	REG_CFG_3C Default : [0x39]	IN_PLL_LPF_CS_PRG_FREQ [7:0]	7:0	R/W	39h	IN_PLL_LPF_CS_PRG_FREQ [23:0]= 7.17 IN_PLL_FREQ = 264MHz/ N.f
0x3D	REG_CFG_3D Default : [0x05]	IN_PLL_LPF_CS_PRG_FREQ [15:8]	7:0	R/W	05h	
0x3E	REG_CFG_3E Default : [0x33]	IN_PLL_LPF_CS_PRG_FREQ [23:16]	7:0	R/W	33h	
0x3F	REG_CFG_3F Default : [0x8d]	IN_PLL_ENABLE_SATBLE_CLK_MODE	7	R/W	1b	Input lpll stable clock mode setting 0 = disable 1 = enable
		IN_PLL_LOCK_IN_GLITCH_CLR_CTRL	6	R/W	0b	Input lpll lock-in glitch clear setting 0 = normal 0->1 = clear IRQ
		IN_PLL_LOCK_IN_IRQ_CLR_CTRL	5	R/W	0b	Input lpll lock-in IRQ clear setting 0 = normal 0->1 = clear IRQ
		IN_PLL_NO_INPUT_IRQ_CLR_CTRL	4	R/W	0b	Input lpll no-input IRQ clear setting 0 = normal 0->1 = clear IRQ
		IN_PLL_ENABLE_IRQ_PLL_LOCK_IN	3	R/W	1b	Input lpll lock-in IRQ setting 0 = disable IRQ 1 = enable IRQ
		IN_PLL_ENABLE_IRQ_PLL_NO_INPUT	2	R/W	1b	Input lpll no-input IRQ setting 0 = disable IRQ

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						1 = enable IRQ
		IN_PLL_ENABLE_PLL_NO_INPUT_AUTO_PRG	1	R/W	0b	Input lpll no-input auto manual frequency setting 0 = normal 1 = no-input manual programming mode
		IN_PLL_ENABLE_LPLL_256FS_SYNTHESIZER	0	R/W	1b	Input lpll enable control 0 = off 1 = on
0x40	REG_CFG_40 Default : [0x12]	IN_PLL_FREQ_LOCK_CURRENT_MODE	7	R/W	0b	Input lpll test mode 0 = normal 1 = lock frequency detector
		IN_PLL_LOCK_FREQ_STATUS_READ	6	R/W	0b	Input lpll frequency status read back 0 = read 1 time 1 = enable continue read back
		IN_PLL_FREQ_PRG_MODE	5	R/W	0b	Input lpll test mode 0 = normal 1 = manual programming mode
		IN_PLL_LOCK_IN_AUTO_SWITCH_BAND_MODE	4	R/W	1b	Input lpll auto switch to low bandwidth if lock-in 0 = high bandwidth mode 1 = auto mode
		IN_PLL_SELECT_FREQ_GAIN[1:0]	3:2	R/W	00b	Input lpll frequency gain setting 00 = min 11 = max
		IN_PLL_SELECT_PHASE_GAIN[1:0]	1:0	R/W	10b	Input lpll phase gain setting 00 = min 11 = max
0x41	REG_CFG_41 Default : [0x39]	OUT_PLL_LPF_CS_PRG_FREQ [7:0]	7:0	R/W	39h	OUT _PLL_LPF_CS_PRG_FREQ [23:0]= 7.17 OUT _PLL_FREQ = 264MHz/ N.f
0x42	REG_CFG_42 Default : [0x05]	OUT _PLL_LPF_CS_PRG_FREQ [15:8]	7:0	R/W	05h	
0x43	REG_CFG_43 Default : [0x33]	OUT _PLL_LPF_CS_PRG_FREQ [23:16]	7:0	R/W	33h	
0x44	REG_CFG_44 Default : [0x8d]	OUT _PLL_ENABLE_SATBLE_CLK_MODE	7	R/W	1b	Output lpll stable clock mode setting 0 = disable 1 = enable
		OUT _PLL_LOCK_IN_GLITCH_CLR_CTRL	6	R/W	0b	Output lpll lock-in glitch clear setting 0 = normal

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
						0->1 = clear IRQ
		OUT _PLL_LOCK_IN_IRQ_CLR_CTRL	5	R/W	0b	Output lpll lock-in IRQ clear setting 0 = normal 0->1 = clear IRQ
		OUT _PLL_NO_INPUT_IRQ_CLR_CTRL	4	R/W	0b	Output lpll no-input IRQ clear setting 0 = normal 0->1 = clear IRQ
		OUT _PLL_ENABLE_IRQ_PLL_LOCK_IN	3	R/W	1b	Output lpll lock-in IRQ setting 0 = disable IRQ 1 = enable IRQ
		OUT _PLL_ENABLE_IRQ_PLL_NO_INPUT	2	R/W	1b	Output lpll no-input IRQ setting 0 = disable IRQ 1 = enable IRQ
		OUT _PLL_ENABLE_PLL_NO_INPUT_AUTO_PRG	1	R/W	0b	Output lpll no-input auto manual frequency setting 0 = normal 1 = no-input manual programming mode
		OUT _PLL_ENABLE_LPLL_256FS_SYNTHESIZER	0	R/W	1b	Output lpll enable control 0 = off 1 = on
0x45	REG_CFG_45 Default : [0x12]	OUT _PLL_FREQ_LOCK_CURRENT_MODE	7	R/W	0b	Output lpll test mode 0 = normal 1 = lock frequency detector
		OUT _PLL_LOCK_FREQ_STATUS_READ	6	R/W	0b	Output lpll frequency status read back 0 = read 1 time 1 = enable continue read back
		OUT _PLL_FREQ_PRG_MODE	5	R/W	0b	Output lpll test mode 0 = normal 1 = manual programming mode
		OUT _PLL_LOCK_IN_AUTO_SWITCH_BAND_MODE	4	R/W	1b	Output lpll auto switch to low bandwidth if lock-in 0 = high bandwidth mode 1 = auto mode
		OUT _PLL_SELECT_FREQ_GAIN[1:0]	3:2	R/W	00b	Output lpll frequency gain setting 00 = min 11 = max
		OUT _PLL_SELECT_PHASE_GAIN[1:0]	1:0	R/W	10b	Output lpll phase gain setting 00 = min

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						11 = max
0x46	REG_CFG_46 Default : [0x00]	NOSYNC_ADC	7	R/W	0b	Down sample FIFO report 0 = normal report 1 = disable function
		NOSYNC_DAC	6	R/W	0b	Up sample FIFO report 0 = normal report 1 = disable function
		RESERVED	5	R/W	0b	
		RESERVED	4	R/W	0b	
		RESERVED	3	R/W	0b	
		RESERVED	2	R/W	0b	
		HB1G	1	R/W	0b	HB1 Gain 0 = -0.00001 dB 1 = -0.05 dB
		LEFT_OUT_ONLY	0	R/W	0b	SRC test_mode 0 = normal 1 = only left channel
0x47	REG_CFG_47 Default : [0x24]	CDR_BYPASS_FINE_LOCK_IN_CHK	7	R/W	0b	SPDIF CDR fine lock in check bypass setting 0 = normal 1 = bypass checking
		CDR_FINE_CMD_CNT_CMP_DC [6:0]	6:0	R/W	10_0100b	SPDIF CDR fine lock in check setting 04h = min 14h = default 3fh = max
0x48	REG_CFG_48 Default : [0x00]	SEL_DIVIDER_CLK_TEST[1:0]	7:6	R/W	00b	Test mode clock output divider 00 = /1 01 = /2 10 = /4 11 = /8
		SEL_CLK_TEST[5:0]	5:0	R/W	0-0000b	Test clock selector 00h = ~~clk_250mhz_osc_post_synthesizer_z~~ 01h = clk_264mhz_mpll_feedback_synthesizer_z 02h = clk_264mhz_mpll_post_synthesizer_z 03h = clk_528mhz_spdif_cdr_256fs_synthesizer_z 04h = clk_264mhz_input_lpll_synthesizer_z 05h = clk_264mhz_output_lpll_synthesizer_z

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						06h = clk_200mhz_src_mf_ratio_synthesizer_z 07h = clk_132mhz_synthesizer_ref_input_spdif_i2s_dsd_z 08h = clk_132mhz_synthesizer_ref_input_src_8_mode_z 09h = clk_132mhz_spdif_rx_128_fs_z 0ah = clk_50mhz_i2s_rx_bclk_z 0bh = clk_25mhz_dsd_rx_bclk_z 0ch = clk_125mhz_input_system_128_fs_z 0dh = clk_125mhz_output_system_128_160_fs_z 0eh = clk_125mhz_spdif_tx_128_160_fs_z 0fh = clk_50mhz_i2s_tx_bclk_48_64_fs_z 10h = clk_25mhz_dsd_tx_bclk_16_4fs_z 11h = clk_8mhz_i2c_z 12h = clk_1mhz_timer_z 13h = clk_16khz_timer_z 14h = clk_1khz_timer_z 15h = clk_50mhz_in_lpll_0_ref_in_z 16h = clk_50mhz_out_lpll_0_ref_in_z 17h = clk_50mhz_out_lpll_1_ref_in_z 18h = clk_50mhz_mpll_ref_in_z 19h = clk_50mhz_mpll_feedback_in_z 1ah = clk_125mhz_filter_mac_dsp_dac_z 1bh = clk_125mhz_src_mac_dsp_z 1ch = clk_16khz_no_input_timer_z 1dh = clk_12mhz_mpll_div_22_z 1eh = clk_125mhz_filter_mac_dsp_adc_z 1fh = CDR_DATA_RESAMPLE_132MHZ_SPDIF_RX_128_FS_z 20h = SPDIF_IN_TEST 21h = clk_25mhz_dsd_pcm2dsd_bclk_16_4fs_z 22h = clk_50mhz_dsd_pcm2dsd_volume_mclk_z 23h = clk_50mhz_i2s_dsd_rx_bclk_auto_detect_z 24h = clk_10hz_timer_z 25h = digital_osc_50mhz_clk_z Others = reserved
0x49	REG_CFG_49 Default : [0x28]	SEL_SRC_BANDWIDTH[1:0]	7:6	R/W	00b	SRC ratio M-code bandwidth 00 = 26-bit 01 = 24-bit 10 = 22-bit

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
						11 = 20-bit
		SEL_KERNEL_TIMER_2[1:0]	5:4	R/W	10b	Select kernel tmer 2 time step for waiting DAC stable 00 = 125 ms 01 = 250 ms 10 =500 ms 11 = 1000 ms
		ENABLE_KERNEL_TIMER_2	3	R/W	1b	Enable kernel timer 2 addition 1 second mute delay for some DAC depop 0 = disable 1 = enable
		SRAM_BIST_MD	2	R/W	0b	Sram test mode 0 = normal 1= sram BIST
		ENABLE_CLK_TEST	1	R/W	0b	Test mode Pin-36 MCLK (pin-24 in 32 QFN) 0 = normal 1 = test clock out
		EXT_REG_ENABLE_BIST	0	R/W	0b	Test mode 0 = normal 1 = force all clock to scan clock
0x4A	REG_CFG_4A Default : [0x41]	FORCE_4P8_SRC_BANDWIDTH	7	R/W	0b	SRC ratio M-code bandwidth test mode 0 = normal 1 = set to 4.8 high bandwidth
		ENABLE_CDR_AUTO_RESET_VC	6	R/W	1b	Enable SPDIF CDR re-lock with reset Vc 0 = disable 1 = enable
		CLR_KERNEL_IRQ	5	R/W	0b	All kernel system IRQ clear setting 0 = normal 0->1 = clear IRQ
		CLR_RESET_IRQ	4	R/W	0b	Power on reset IRQ clear setting 0 = normal 0->1 = clear IRQ
		FORCE_VIRTUAL_768KHZ	3	R/W	0b	Kernel system virtual 768KHz test mode 0 = disable 1 = enable
		FORCE_ENABLE_ALL_RX	2	R/W	0b	Force enable all Rx front end 0 = normal

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						1 = force clock on
		FORCE_KERNEL_FREE_RUN	1	R/W	0b	Kernel system force free run 0 = normal 1 = free run no de-pop
		ENABLE_KERNEL_AUTO_MUTE	0	R/W	1b	Kernel system auto mute setting 0 = disable 1 = enable
0x4B	REG_CFG_4B Default : [0xb0]	SEL_BIT_ERR_CNT[1:0]	7:6	R/W	10b	SPDIF CDR bit error rate range setting 00 = 1 / 512 01 = 2 / 512 10 = 4 / 512 11 = 6 / 512
		ENABLE_CHK_OUTPUT_LOCK_IN	5	R/W	1b	Kernel stable check output pll lock in status 0 = un-checked 1 = checked
		ENABLE_CHK_INPUT_LOCK_IN	4	R/W	1b	Kernel stable check input pll lock in status 0 = un-checked 1 = checked
		ENABLE_AUTO_TIMING_RE_SYNC_OUTPUT_DSD	3	R/W	0b	Output DSD timing generator auto re-sync control 0 = disable 1 = enable
		ENABLE_AUTO_TIMING_RE_SYNC_OUTPUT_I2S	2	R/W	0b	Output I2S timing generator auto re-sync control 0 = disable 1 = enable
		ENABLE_AUTO_TIMING_RE_SYNC_OUTPUT_SRC	1	R/W	0b	Output SRC timing generator auto re-sync control 0 = disable 1 = enable
		ENABLE_AUTO_TIMING_RE_SYNC_INPUT_SRC	0	R/W	0b	Input SRC timing generator auto re-sync control 0 = disable 1 = enable
0x4C	REG_CFG_4C Default : [0x90]	DEFINE_PIN_DSD_IN_CH7	7	R/W	1b	Channel 7 input definition (I2S_DSD_IN_2) 0 = i2s pin assignment 1 = dsd pin assignment
		DEFINE_PIN_DSD_IN_CH6	6	R/W	0b	Channel 6 input definition (I2S_DSD_IN_1) 0 = i2s pin assignment 1 = dsd pin assignment

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
		DEFINE_PIN_DSD_IN_CH5	5	R/W	0b	Channel 5 input definition (I2S_DSD_IN_0) 0 = i2s pin assignment 1 = dsd pin assignment
		ENABLE_AUTO_I2S_DSD_DETECT	4	R/W	1b	Channel 5,6,7 I2S/DSD auto detector (I2S_DSD_IN_[2:0]) 0 = manual mode 1 = auto detecting While auto detecting mode, if error, I2S/DSD input setting will become manual mode setting.
		SET_MANUAL_D2P_FREQ	3	R/W	0b	Set DSD to PCM output fix ratio manual mode, active setting. 0 = fix auto mode 1 = manual mode
		DSD2PCM_MANUAL_D2P_FREQ[2:0]	2:0	R/W	000b	DSD to PCM output fix ratio manual setting 000 = 1 x fs 001 = 2 x fs 010 = 4 x fs 011 = 8 x fs 100 = 16 x fs Others = reserved
0x4D	REG_CFG_4D Default : [0x35]	RELOAD_POWER_ON_LATCH	7	R/W	0b	Re-do power on latch 0->1 = latch again
		INV_I2S_TX_SLAVE_MODE	6	R/W	0b	Inverse power on latch I2S slave mode setting 0 = follow power on latch 1 = inverse power on latch
		VOLUME_SHIFT_GAIN[1:0]	5:4	R/W	11b	PCM volume control shift gain setting 00 = +0dB 01 = +6dB 10 = +12dB 11 = +18dB
		SPDIF_DIRECT_OUT	3	R/W	0b	SPDIF OUTPUT Pin pass through setting 0 = normal 1 = Rx -> Tx pass through
		D2P_SHIFT_GAIN_2X	2	R/W	1b	DSD to PCM comb filter normalize +6dB gain 0 = 0dB 1 = +6dB
		NEW_COARSE_OFFSET_MODE	1	R/W	0b	SPDIF CDR new coarse offset mode 0 = disable

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						1 = enable
		D2P_NEW_SRC_MODE	0	R/W	1b	DSD to PCM with new SRC mode, active setting. 0 = disable 1 = enable If enable this function, ENABLE_DOP_TO_PCM will auto enable.
0x4E	REG_CFG_4E Default : [0x44]	RESERVED	7	R/W	0b	
		OUT_PLL_LOW_BAND_WIDTH_N_256	6	R/W	1b	Output pll input reference divider fix /256 0 = normal 1 = /256
		OUT_PLL_LOW_BAND_WIDTH_FREQ	5	R/W	0b	Output pll loop bandwidth frequency setting 0 = normal 1 = low bandwidth
		OUT_PLL_LOW_BAND_WIDTH_PHASE	4	R/W	0b	Output pll loop bandwidth phase setting 0 = normal 1 = low bandwidth
		RESERVED	3	R/W	0b	
		IN _PLL_LOW_BAND_WIDTH_N_256	2	R/W	1b	Input pll input reference divider fix /256 0 = normal 1 = /256
		IN _PLL_LOW_BAND_WIDTH_FREQ	1	R/W	0b	Input pll loop bandwidth frequency setting 0 = normal 1 = low bandwidth
		IN_PLL_LOW_BAND_WIDTH_PHASE	0	R/W	0b	Input pll loop bandwidth phase setting 0 = normal 1 = low bandwidth
0x4F	REG_CFG_4F Default : [0x06]	CDR_LPF_CS_PRG_FREQ_ext_msb	7	R/W	0b	CDR_LPF_CS_PRG_FREQ[20] = CDR_LPF_CS_PRG_FREQ_ext_msb CDR_LPF_CS_PRG_FREQ[20:0] = 8.13 SPDIF CDR CLOCK = 528MHz/ N.f
		SET_8KHZ_4X_FS_I2S	6	R/W	0b	Patch BT 8khz input from i2s 0 = normal 1 = patch 8khz *4
		SET_8KHZ_4X_FS_SPDIF	5	R/W	0b	Patch BT 8khz input from spdif 0 = normal 1 = patch 8khz *4
		SPDIF_TX_CLR_STATUS_TIMING_RE_SYNC	4	R/W	0b	SPDIF output Timing generator re-sync signal status clear

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
						0 = normal 0->1 = clear
		ENABLE_AUTO_TIMING_RE_SYNC_OUTPUT_SPDIF	3	R/W	0b	Output SPDIF timing generator auto re-sync control 0 = disable 1 = enable
		ENABLE_POWER_DOWN_TRISTATE	2	R/W	1b	Power down all, output pin tri-state setting 0 = normal 1 = tri-state
		AUTO_8KHZ_4X_FS_SPDIF_CLK_DIV2	1	R/W	1b	Patch BT 8khz input from spdif, auto clock divider 2 0 = manual 1 = auto
		INV_CLK_50MHZ_I2S_DSD_RX_BCLK_AUTO_DETECT	0	R/W	0b	Inverse CLK_50MHZ_I2S_DSD_RX_BCLK_AUTO_DETECT clock system 0 = normal 1 = inverse
0x50	REG_CFG_50 Default : [0x00]	N_F_TABLE_32K_FREQ [7:0]	7:0	R/W	00h	MPLL post synthesizer 32k gen. n.f divider N_F_TABLE_32K_FREQ [23:0]= 5.19 OUT _FREQ = MPLL(288MHz)/ N.f
0x51	REG_CFG_51 Default : [0xa0]	N_F_TABLE_32K_FREQ [15:8]	7:0	R/W	a0h	
0x52	REG_CFG_52 Default : [0x8c]	N_F_TABLE_32K_FREQ [23:16]	7:0	R/W	8ch	
0x53	REG_CFG_53 Default : [0x73]	N_F_TABLE_44K _FREQ [7:0]	7:0	R/W	73h	MPLL post synthesizer 44k gen. n.f divider N_F_TABLE_44K _FREQ [23:0]= 5.19 OUT _FREQ = MPLL(288MHz)/ N.f
0x54	REG_CFG_54 Default : [0x0a]	N_F_TABLE_44K _FREQ [15:8]	7:0	R/W	0ah	
0x55	REG_CFG_55 Default : [0x66]	N_F_TABLE_44K_FREQ [23:16]	7:0	R/W	66h	
0x56	REG_CFG_56 Default : [0x00]	N_F_TABLE_48K _FREQ [7:0]	7:0	R/W	00h	MPLL post synthesizer 48k gen. n.f divider N_F_TABLE_48K _FREQ [23:0]= 5.19 OUT _FREQ = MPLL(288MHz)/ N.f
0x57	REG_CFG_57 Default : [0xc0]	N_F_TABLE_48K _FREQ [15:8]	7:0	R/W	c0h	
0x58	REG_CFG_58 Default : [0x5d]	N_F_TABLE_48K_FREQ [23:16]	7:0	R/W	5dh	
0x59	REG_CFG_59 Default : [0x21]	CLR_STATUS_TIMING_RE_SYNC_PCM2DSD	7	R/W	0b	PCM to DSD Timing generator re-sync signal status clear 0 = normal 0->1 = clear

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
		ENABLE_AUTO_TIMING_RE_SYNC_PCM2DSD	6	R/W	0b	PCM to DSD timing generator auto re-sync control 0 = disable 1 = enable
		SEL_TX_PAD_DSD_SPEC	5	R/W	1b	I2S_DSD_0 Tx pin definition setting [pin 22,23,24] 0 = set to I2S specification 1 = set to DSD specification
		SEL_TX_PAD_I2S_SPEC	4	R/W	0b	I2S_DSD_1 Tx pin definition setting [pin 31,32,33] 0 = set to I2S specification 1 = set to DSD specification If I2S Tx port is set to slave mode, this port is only support I2S specification. This is auto setting.
		SEL_NEW_P2D_DSD_MODE[1:0]	3:2	R/W	00b	PCM to DSD mode, DSD output ratio setting 00 = dsd 1x mode 01 = dsd 2x mode 10 = dsd 4x mode 11 = dsd 8x mode If SET_NEW_P2D_DSD_DOP_MODE =1, DSD+DoP output only support up to 4x mode. If SET_NEW_P2D_DSD_DOP_MODE =0, DSD+PCM output support up to 8x mode. But, DSD will be dominated by PCM setting. Please refer to DSD/DoP/PCM limitation table
		SET_NEW_P2D_DSD_DOP_MODE	1	R/W	0b	PCM to DSD mode, function selection, output format setting 0 = DSD + PCM output 1 = DSD + DoP output
		SET_NEW_P2D_MODE	0	R/W	1b	Set PCM to DSD mode active 0 = disable 1 = enable while src mode 01234 If enable this function, D2P_NEW_SRC_MODE will auto enable.
0x5A	REG_CFG_5A Default : [0x1f]	ENABLE_CLK_25MHZ_DSD_PCM2DSD_BCLK_16_4FS	7	R/W	0b	Force clock enable 0 = auto 1 = force on
		ENABLE_CLK_50MHZ_DSD_PCM2DSD_VOLUME_MCLK	6	R/W	0b	Force clock enable 0 = auto

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						1 = force on
		PCM2DSD_SAMPLE_LR_CHANGE	5	R/W	0b	PCM to DSD sample left/right swap 0 = normal 1 = swap
		PCM2DSD_FORCE_MUTE	4	R/W	1b	PCM to DSD volume mute control 0 = normal 1 = force mute
		SET_RIGHT_VOLUME_EQ_LEFT_P2D	3	R/W	1b	PCM to DSD volume control mode setting 0 = independent 1 = right channel is equal to left channel
		SET_VOLUME_P2D_EQ_PCM	2	R/W	1b	PCM to DSD volume control mode setting 0 = independent 1 = follow PCM volume control
		REG_CLK_LOW_FREQ_MODE_4567	1	R/W	1b	Low frequency output setting SRC mode-4,5,6,7 0 = normal output 32k ~ 768k Hz 1 = under 32kHz
		REG_CLK_LOW_FREQ_MODE_3	0	R/W	1b	Low frequency output setting SRC mode-3 0 = normal output 32k ~ 768k Hz 1 = under 32kHz
0x5B	REG_CFG_5B Default : [0x00]	VOLUME_VALUE_RIGHT_P2D [3:0]	7:4	R/W	0000b	PCM to DSD Volume control right channel [3:0]
		VOLUME_VALUE_LEFT_P2D [3:0]	3:0	R/W	0000b	PCM to DSD Volume control left channel [3:0]
0x5C	REG_CFG_5C Default : [0x24]	VOLUME_VALUE_LEFT_P2D [11:4]	7:0	R/W	24h	PCM to DSD Volume control left channel [11:0] (step -0.03125dB) Offset S.dB = VOLUME_SHIFT_GAIN_PCM2DSD[1:0] 000h = 0 dB +S.dB 001h = -0.03125 dB +S.dB 240h = -18 dB +S.dB ….. FEF = -127.96875 dB +S.dB FFxh = mute
0x5D	REG_CFG_5D Default : [0x24]	VOLUME_VALUE_RIGHT_P2D [11:4]	7:0	R/W	24h	PCM to DSD Volume control right channel [11:0] (step -0.03125dB) Offset S.dB = VOLUME_SHIFT_GAIN_PCM2DSD[1:0] 000h = 0 dB +S.dB 001h = -0.03125 dB +S.dB 240h = -18 dB +S.dB ….. FEF = -127.96875 dB +S.dB

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						FFxh = mute If : SET_RIGHT_VOLUME_EQ_LEFT_P2D = 1 Then : VOLUME_VALUE_ RIGHT_P2D = VOLUME_VALUE_LEFT_P2D
0x5E	REG_CFG_5E Default : [0x34]	BYPASS_VOLUME_PCM2DSD	7	R/W	0b	Bypass PCM to DSD volume test mode control function 0 = normal 1 = bypass volume control, only for test
		SW_FORCE_MUTE_PIN	6	R/W	0b	Software control STATUS output pin for mute 0 = auto 1 = force mute
		VOLUME_SHIFT_GAIN_PCM2DSD[1:0]	5:4	R/W	11b	PCM to DSD volume control shift gain setting 00 = +0dB 01 = +6dB 10 = +12dB 11 = +18dB
		VOLUME_CMP_PERIOD_PCM2DSD[3:0]	3:0	R/W	0100b	PCM to DSD Volume control DSP step N-sample Command period = N + 1 sample
0x5F	REG_CFG_5F Default : [0x6b]	RESERVED	7	R/W	0b	
		ENABLE_DELTA_SIGMA_UP_RESAMPLE	6	R/W	1b	Delta sigma up sample control 0 = disable 1 = enable
		SET_CLR_FEEDBACK_DELTA_SIGMA_AUTO	5	R/W	1b	PCM to DSD sigma delta mute auto clear 0 = disable 1 = auto
		CLR_FEEDBACK_DELTA_SIGMA	4	R/W	0b	Delta sigma feedback clear 0 = normal 1 = clr
		SET_DOWN_6DB_PCM2DSD	3	R/W	1b	PCM to DSD -6dB gain setting 0 = 0 dB 1 = -6 dB
		SEL_NORMALIZE_GAIN [2:0]	2:0	R/W	011b	PCM to DSD sigma delta gain setting 0 = -0 dB (min) 1 = -0.25 dB 2 = -0.5 dB 3 = -0.75 dB

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						4 = -1.0 dB 5 = -1.25 dB 6 = -1.5 dB 7 = -1.75 dB (max)
0x60	REG_CFG_60 Default : [0x07]	RESERVED	7	R/W	0b	
		SILENCE_DETECT_LEN_PCM[2:0]	6:4	R/W	000b	Input PCM silence detect timer selection 0h = disable 1h = 0.1 second 2h = 0.5 second 3h = 1 second 4h =2 second 5h = 4 second 6h = 8 second 7h = 16 second
		RESERVED	3	R/W	0b	
		SILENCE_DETECT _MSB_PCM[2:0]	2:0	R/W	111b	Input PCM silence detect active sample selection 0h = 14 bits 1h = 16 bits 2h = 18 bits 3h = 20 bits 4h = 22 bits 5h = 24 bits 6h = 28 bits 7h = 32 bits
0x61	REG_CFG_61 Default : [0x20]	SEL_DIGITAL_OSC_FREQ[7:0]	7:0	R/W	20h	Digital OSC frequency selection Frequency = 1 / (12ns + (250ps * SEL_DIGITAL_OSC_FREQ))
0x62	REG_CFG_62 Default : [0x02]	SPDIF_NON_PCM_MUTE_NOT_MODE7	7	R/W	0b	SPDIF input non-pcm mode setting, while non-pcm setting to mute 0 = bypass mode7 & mute 1 = current mode & mute
		OUT_LPLL_1_DE_JITTER	6	R/W	0b	Analog PLL internal test mode 0 = normal 1 = enable test mode for de-jitter
		OUT_LPLL_0_DE_JITTER	5	R/W	0b	Analog PLL internal test mode 0 = normal 1 = enable test mode for de-jitter

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
		IN_LPLL_DE_JITTER	4	R/W	0b	Analog PLL internal test mode 0 = normal 1 = enable test mode for de-jitter
		I2S_RX_XCHG_LR	3	R/W	0b	I2S Rx left, right channel exchange 0 = normal 1 = exchange
		I2S_TX_XCHG_LR	2	R/W	0b	I2S Tx left, right channel exchange 0 = normal 1 = exchange
		FORCE_DIGITAL_OSC_50MHZ_ON	1	R/W	1b	Force digital OSC always on 0 = auto mode 1 = force on
		SEL_OSC_SOURCE	0	R/W	0b	Internal OSC source selection 0 = analog OSC 1 = digital OSC
0x63	REG_CFG_63 Default : [0x00]	RESERVED	7:0	R/W	00h	
0x9F	REG_CFG_9F Default : [0x00]	RESERVED	7:2	R/W	0000-00b	
		RESET_ALL	1	R/W	0b	Reset chipset 0 = normal 1 = reset all system but register table
		RESTART_ALL	0	R/W	0b	Re-power-on chipset 0 = normal 1 = re-start all system including register table reset
STATUS REGISTER						
0x70	REG_STATUS_70 Default : [0x00]	POWER_ON_LATCH_DC[7] = SPDIF support up to 32 bit	7	R	0b	BONDING_IN_0 SPDIF support up to 32 bit 0 = 24 bits 1 = 32 bits
		POWER_ON_LATCH_DC[6:5] = I2C_ID[1:0]	6:5	R	00b	I2C serial interface device ID selection 00 = 0x20 01 = 0x22 10 = 0x24 11 = 0x26
		POWER_ON_LATCH_DC[4:3] = SEL_XTAL[1:0]	4:3	R	00b	Select Crystal frequency 00 = 12MHz

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						01 = 11.2896MHz 10 = 12.288MHz 11 = 14.318MHz
		POWER_ON_LATCH_DC[2] = Reserved	2	R	0b	Reserved
		POWER_ON_LATCH_DC[1] = SEL_I2S_TX_SLAVE_MODE	1	R	0b	Select I2S Tx Slave / Master mode 0 = master 1 = slave Pin [31], [32], [33] support I2S Master/Slave mode.
		POWER_ON_LATCH_DC[0] = Reserved	0	R	0b	Reserved
0x71	REG_STATUS_71 Default : [0x00]	RESERVED	7:4	R	0000b	
		POWER_ON_LATCH_DC[11] = Support PCM to DSD SRC mode	3	R	0b	BONDING_IN_3 Support PCM to DSD SRC mode 0 = not support 1 = support
		POWER_ON_LATCH_DC[10] = Support DSD to PCM SRC mode	2	R	0b	BONDING_IN_2 Support DSD to PCM SRC mode 0 = not support 1 = support
		POWER_ON_LATCH_DC[9] = SPDIF support up to 768khz	1	R	0b	BONDING_IN_1 SPDIF support up to 768khz 0 = 384 KHz 1 = 768 KHz
		POWER_ON_LATCH_DC[8] = SPDIF support up to 384khz	0	R	0b	BONDING_IN_4 SPDIF support up to 384khz 0 = 192 KHz 1 = 384 KHz
0x72	REG_STATUS_72 Default : [0x00]	SPDIF_RX_CH_STATUS[7:0]	7:0	R	00h	SPDIF Rx channel status[39:0] Refer to the IEC 60958-3
0x73	REG_STATUS_73 Default : [0x00]	SPDIF_RX_CH_STATUS[15:8]	7:0	R	00h	
0x74	REG_STATUS_74 Default : [0x00]	SPDIF_RX_CH_STATUS[23:16]	7:0	R	00h	
0x75	REG_STATUS_75 Default : [0x00]	SPDIF_RX_CH_STATUS[31:24]	7:0	R	00h	
0x76	REG_STATUS_76 Default : [0x00]	SPDIF_RX_CH_STATUS[39:32]	7:0	R	00h	

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
0x77	REG_STATUS_77 Default : [0x00]	I2S_RX_32BIT	7	R	0b	I2S Rx 32 bits detector 0 = others 1 = 32 bits data rate
		SPDIF_RX_32BIT	6	R	0b	SPDIF Rx 32 bits detector 0 = 24 bits data rate 1 = 32 bits data rate
		I2S_RX_DOP_MODE	5	R	0b	I2S Rx DoP detector 0 = non-DoP 1 = DoP
		SPDIF_RX_DOP_MODE	4	R	0b	SPDIF Rx DoP detector 0 = non-DoP 1 = DoP
		SPDIF_RX_DE_EMPHASIS_FLAG	3	R	0b	SPDIF Rx de-emphasis detector 0 = normal 1 = de-emphasis
		SPDIF_RX_NON_PCM_FLAG	2	R	0b	SPDIF Rx non-pcm detector 0 = normal 1 = non-pcm
		AUTO_FADING_STATUS	1	R	0b	Fading control direction status 0 = fading out 1 = fading in
		CTRL_MUTE_FADING_DONE	0	R	0b	Fading control finished status 0 = busy 1 = done
0x78	REG_STATUS_78 Default : [0x00]	KERNEL_IRQ_STATUS mode_chg_124816_Q	7	R	0b	Status mode_chg_124816_Q 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS mode_chg_src_Q	6	R	0b	Status mode_chg_src_Q 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS mode_chg_dop_in_Q	5	R	0b	Status mode_chg_dop_in_Q 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS mode_chg_non_pcm_Q	4	R	0b	Status mode_chg_non_pcm_Q 1 = IRQ flag 0 = normal

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
		KERNEL_IRQ_ STATUS in_pll_lock_in	3	R	0b	Status in_pll_lock_in 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS out_pll_lock_in	2	R	0b	Status out_pll_lock_in 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS in_pll_no_input	1	R	0b	Status in_pll_no_input 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS out_pll_no_input	0	R	0b	Status out_pll_no_input 1 = IRQ flag 0 = normal
0x79	REG_STATUS_79 Default : [0x00]	RESERVED	7	R	0b	
		RESERVED	6	R	0b	
		STATUS_CTRL_SYSTEM_RESET_IRQ	5	R	0b	Status power on reset 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS cmp_mode_chg_de_emphasis_Q	4	R	0b	Status cmp_mode_chg_de_emphasis_Q 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS mode_chg_dop_to_pcm_Q	3	R	0b	Status mode_chg_dop_to_pcm_Q 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS mode_chg_spdif_rx_32_Q	2	R	0b	Status mode_chg_spdif_rx_32_Q 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS mode_chg_input_channel_Q	1	R	0b	Status mode_chg_input_channel_Q 1 = IRQ flag 0 = normal
		KERNEL_IRQ_ STATUS mode_chg_freq_Q	0	R	0b	Status mode_chg_freq_Q 1 = IRQ flag 0 = normal
0x7A	REG_STATUS_7A Default : [0x00]	PCM_SILENCE_BOTH_FLAG	7	R	0b	Input PCM silence detect left and right channels flag 0 = normal 1= silence detected
		PCM_SILENCE_R_FLAG	6	R	0b	Input PCM silence detect right channel flag

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
						0 = normal 1= silence detected
		PCM_SILENCE_L_FLAG	5	R	0b	Input PCM silence detect left channel flag 0 = normal 1= silence detected
		CTRL_I2SZ_DSD_ERROR_DETECTED	4	R	0b	Channel 5,6,7 auto detect I2S/DSD 0 = normal 1 = error flag While auto detecting mode, if error, I2S/DSD input setting will become manual mode setting.
		CTRL_I2SZ_DSD_DETECTED	3	R	0b	Channel 5,6,7 auto detect I2S/DSD 0 = I2S 1 = DSD
		CTRL_AUTO_SEL_MPLL_50MHZ_SOURCE	2	R	0b	Mpll reference clock status 0 = OSC 50MHz 1 = Xtal 12MHz
		CTRL_SET_DOP_OUT	1	R	0b	DoP flag output data format 0 = not DoP 1 = DoP
		PAD_STATUS_MUTE_OUT	0	R	0b	Output status mute signal 0 = low 1 = high
0x7B	REG_STATUS_7B Default : [0x00]	ADC_FIFOL_OV	7	R	0b	SRC down sample FIFO flag left channel 0 = normal 1 = over run
		ADC_FIFOL_UR	6	R	0b	SRC down sample FIFO flag left channel 0 = normal 1 = under run
		ADC_FIFOR_OV	5	R	0b	SRC down sample FIFO flag right channel 0 = normal 1 = over run
		ADC_FIFOR_UR	4	R	0b	SRC down sample FIFO flag right channel 0 = normal 1 = under run
		DAC_FIFOL_OV	3	R	0b	SRC up sample FIFO flag left channel 0 = normal

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
						1 = over run
		DAC_FIFOL_UR	2	R	0b	SRC up sample FIFO flag left channel 0 = normal 1 = under run
		DAC _FIFOR_OV	1	R	0b	SRC up sample FIFO flag right channel 0 = normal 1 = over run
		DAC _FIFOR_UR	0	R	0b	SRC up sample FIFO flag right channel 0 = normal 1 = under run
0x7C	REG_STATUS_7C Default : [0x00]	RESERVED	7	R	0b	
		RESERVED	6	R	0b	
		RESERVED	5	R	0b	
		RESERVED	4	R	0b	
		RESERVED	3	R	0b	
		RESERVED	2	R	0b	
		SRC_SRAM_PASS	1	R	0b	SRAM BIST flag 0 = fail 1 = pass
		SRC_SRAM_FINISH	0	R	0b	SRAM BIST flag 0 = busy 1 = done
0x7D	REG_STATUS_7D Default : [0x00]	CTRL_SRC_MF_RATIO[7:0]	7:0	R	00h	SRC in/out Ratio report 4.20
0x7E	REG_STATUS_7E Default : [0x00]	CTRL_SRC_MF_RATIO[15:8]	7:0	R	00h	
0x7F	REG_STATUS_7F Default : [0x00]	CTRL_SRC_MF_RATIO[23:16]	7:0	R	00h	
0x80	REG_STATUS_80 Default : [0x00]	STATUS_SPDIF_CDR_FREQ [7:0]	7:0	R	00h	SPDIF CDR lock frequency report [8.13]
0x81	REG_STATUS_81 Default : [0x00]	STATUS_SPDIF_CDR_FREQ [15:8]	7:0	R	00h	
0x82	REG_STATUS_82 Default : [0x00]	STATUS_SPDIF_CDR_FREQ [20:16]	4:0	R	00h	
		RESERVED	7:5	R	0000b	
0x83	REG_STATUS_83 Default : [0x00]	STATUS_IN_PLL_256FS_FREQ [7:0]	7:0	R	00h	Input pll locked frequency report 8.17

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
0x84	REG_STATUS_84 Default : [0x00]	STATUS_IN_PLL_256FS_FREQ [15:8]	7:0	R	00h	
0x85	REG_STATUS_85 Default : [0x00]	STATUS_IN_PLL_256FS_FREQ [23:16]	7:0	R	00h	
0x86	REG_STATUS_86 Default : [0x00]	STATUS_ OUT _PLL_256FS_FREQ [7:0]	7:0	R	00h	Output pll locked frequency report 7.17
0x87	REG_STATUS_87 Default : [0x00]	STATUS_ OUT _PLL_256FS_FREQ [15:8]	7:0	R	00h	
0x88	REG_STATUS_88 Default : [0x00]	STATUS_OUT_PLL_256FS_FREQ [23:16]	7:0	R	00h	
0x89	REG_STATUS_89 Default : [0x00]	CTRL_IN_PLL_256FS_LOCK_IN_FAST	7	R	0b	Input pll lock in flag 0 = un-locked 1 = locked
		RESERVED	6	R	0b	
		STATUS_IN_PLL_256FS_FREQ_32_44_48[1:0]	5:4	R	0b	Input pll lock frequency table status 00 = 32k x 01 = 44.1k x 10 = 48k x 11 = reserved
		STATUS_IN_PLL_256FS_FREQ_ENCODE[3:0]	3:0	R	0b	Input pll lock frequency table status 0 = 32k 1 = 32k 2 = 44.1k 3 = 48k 4 = 64k 5 = 88.2k 6 = 96k 7 = 128k 8 = 176.4k 9 = 192k A = 256k B = 352.8k C = 384k D = 512k E = 705.6k F = 768k

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
0x8A	REG_STATUS_8A Default : [0x00]	CTRL_OUT_PLL_256FS_LOCK_IN_FAST	7	R	0b	Output pll lock in flag 0 = un-locked 1 = locked
		RESERVED	6	R	0b	
		STATUS_OUT_PLL_256FS_FREQ_32_44_48[1:0]	5:4	R	0b	Output pll lock frequency table status 00 = 32k x 01 = 44.1k x 10 = 48k x 11 = reserved
		STATUS_ OUT _PLL_256FS_FREQ_ENCODE[3:0]	3:0	R	0b	Output pll lock frequency table status 0 = 32k 1 = 32k 2 = 44.1k 3 = 48k 4 = 64k 5 = 88.2k 6 = 96k 7 = 128k 8 = 176.4k 9 = 192k A = 256k B = 352.8k C = 384k D = 512k E = 705.6k F = 768k
0x8B	REG_STATUS_8B Default : [0x00]	CTRL_OUT_PLL_ENABLE_ASRC_DSP	7	R	0b	SRC function status report 0 = bypass SRC 1 = enable SRC
		CTRL_OUT_PLL_SRC_DOWN_124816X[2:0]	6:4	R	000b	SRC function status report 000 = down sample 1x 001 = down sample 2x 010 = down sample 4x 011 = down sample 8x 100 = down sample 16x others = reserved
		CTRL_ENABLE_ASRC_DSP_CLK	3	R	0b	SRC function status report

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						0 = stop 1 = enable
		CTRL_OUT_PLL_SRC_UP_124816X[2:0]	2:0	R	000b	SRC function status report 000 = up sample 1x 001 = up sample 2x 010 = up sample 4x 011 = up sample 8x 100 = up sample 16x others = reserved
0x8C	REG_STATUS_8C Default : [0x00]	CTRL_HOLD_IN_PLL	7	R	0b	Auto de-pop status 0 = normal 1 = hold input pll (fading out)
		STATUS_OUT_PLL_256FS_LOCK_IN_CHG_IRQ	6	R	0b	Output pll lock in status change IRQ flag 0 = normal 1 = IRQ
		STATUS_IN_PLL_256FS_LOCK_IN_CHG_IRQ	5	R	0b	Input pll lock in status change IRQ flag 0 = normal 1 = IRQ
		STATUS_SPDIF_CDR_LOCK_IN_CHG_IRQ	4	R	0b	SPDIF CDR lock in status change IRQ flag 0 = normal 1 = IRQ
		CTRL_SMAPLE_HOLD_DATA	3	R	0b	Auto de-pop status 0 = normal 1 = hold input data (mute)
		STATUS_OUT_PLL_256FS_NO_INPUT_IRQ	2	R	0b	Output pll no input IRQ flag 0 = normal 1 = IRQ
		STATUS_IN_PLL_256FS_NO_INPUT_IRQ	1	R	0b	Input pll no input IRQ flag 0 = normal 1 = IRQ
		STATUS_SPDIF_CDR_NO_INPUT_IRQ	0	R	0b	SPDIF CDR no input IRQ flag 0 = normal 1 = IRQ
0x8D	REG_STATUS_8D Default : [0x00]	DSD_TX_STATUS_TIMING_RE_SYNC	7	R	0b	DSD Tx timing generator stable flag 0 = no auto re-synchronous 1 = re-synchronous event

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
		I2S_TX_STATUS_TIMING_RE_SYNC	6	R	0b	I2S Tx timing generator stable flag 0 = no auto re-synchronous 1 = re-synchronous event
		OUT_SRC_STATUS_TIMING_RE_SYNC	5	R	0b	SRC output & SPDIF Tx timing generator stable flag 0 = no auto re-synchronous 1 = re-synchronous event
		IN_SRC_STATUS_TIMING_RE_SYNC	4	R	0b	SRC input timing generator stable flag 0 = no auto re-synchronous 1 = re-synchronous event
		SPDIF_TX_STATUS_TIMING_RE_SYNC	3	R	0b	SPDIF Tx timing generator stable flag 0 = no auto re-synchronous 1 = re-synchronous event
		STATUS_OUT_PLL_256FS_LOCK_IN_GLITCH	2	R	0b	Output pll lock in stable flag 0 = normal 1 = locked un-stable
		STATUS_IN_PLL_256FS_LOCK_IN_GLITCH	1	R	0b	Input pll lock in stable flag 0 = normal 1 = locked un-stable
		STATUS_SPDIF_CDR_LOCK_IN_GLITCH	0	R	0b	SPDIF CDR lock in stable flag 0 = normal 1 = locked un-stable
0x8E	REG_STATUS_8E Default : [0x00]	SPDIF_RX_ERROR	7	R	0b	
		CTRL_OUT_PLL_256FS_NO_INPUT	6	R	0b	Output pll no input signal flag 0 = normal 1 = no input
		CTRL_IN_PLL_256FS_NO_INPUT	5	R	0b	Input pll no input signal flag 0 = normal 1 = no input
		CTRL_SPDIF_CDR_NO_INPUT	4	R	0b	SPDIF CDR no input signal flag 0 = normal 1 = no input
		STATUS_BLOCK_LOCKED	3	R	0b	SPDIF Rx block lock in flag 0 = un-locked 1 = locked
		CTRL_OUT_PLL_256FS_LOCK_IN	2	R	0b	Output pll lock in flag 0 = un-locked

REGISTER TABLE

Index	Mnemonic	Field Name	Bit	Type	Default	Description
						1 = locked
		CTRL_IN_PLL_256FS_LOCK_IN	1	R	0b	Input pll lock in flag 0 = un-locked 1 = locked
		CTRL_SPDIF_CDR_LOCK_IN	0	R	0b	SPDIF CDR lock in flag 0 = un-locked 1 = locked
0x8F	REG_STATUS_8F Default : [0x00]	RESERVED	7	R	0b	
		~~PIN_SEL_INPUT_CHANNEL[2:0]~~	~~6:4~~	~~R~~	~~000b~~	~~Status of input channel selection~~
		~~PIN_SEL_SRC_FREQ[3:0]~~	~~3:0~~	~~R~~	~~0000b~~	~~Status of output frequency / ratio selection~~
0x90	REG_STATUS_90 Default : [0x00]	PCM2DSD_NON_ZERO_CROSS_STATUS	7	R	0b	PCM to DSD non-zero crossing detect 0 = normal 1 = non-zero crossing
		PCM_NON_ZERO_CROSS_STATUS	6	R	0b	PCM non-zero crossing detect 0 = normal 1 = non-zero crossing
		CTRL_SEL_P2D_DSD_MODE_CLAMP[1:0]	5:4	R	00b	PCM to DSD new SRC mode ratio setting 00 = dsd 1x mode 01 = dsd 2x mode 10 = dsd 4x mode 11 = dsd 8x mode
		RESERVED	3	R	0b	
		STATUS_TIMING_RE_SYNC_PCM2DSD	2	R	0b	PCM to DSD timing generator stable flag 0 = no auto re-synchronous 1 = re-synchronous event
		PCM2DSD_AUTO_FADING_STATUS	1	R	0b	PCM to DSD Fading control direction status 0 = fading out 1 = fading in
		CTRL_MUTE_FADING_DONE_PCM2DSD	0	R	0b	PCM to DSD Fading control finished status 0 = busy 1 = done
0x91	REG_STATUS_91 Default : [0x00]	Device ID	7:0	R	10h	Device ID
0x92	REG_STATUS_92 Default : [0x00]	RESERVED	7:0	R	00h	
0x93	REG_STATUS_93	RESERVED	7:0	R	00h	

REGISTER TABLE						
Index	**Mnemonic**	**Field Name**	**Bit**	**Type**	**Default**	**Description**
	Default : [0x00]					
0x94	REG_STATUS_94 Default : [0x00]	RESERVED	7:0	R	00h	
0x95	REG_STATUS_95 Default : [0x00]	RESERVED	7:0	R	00h	
0x96	REG_STATUS_96 Default : [0x00]	RESERVED	7:0	R	00h	
0x97	REG_STATUS_97 Default : [0x00]	RESERVED	7:0	R	00h	