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Firmware Quickly Start

CT7302 serial chip is an easy control audio bridge chip. Most general audio system just need set the suggest ininital setting value is enough. The chip can auto converter the expect signal to output port. User can reference the following table to initial this chip step by step.

Reset internal MPLL

The chip internal MPLL need software toggle procedure to reset this block after chip is power on.

Register Address 0x2B[3] set to 1
Delay 1 ms
Register Address 0x2B[3] clear to 0

Chip Initial setting value

For input signal compatibility, the following setting values are strongly recommended to write into registers after reset internal MPLL.

Address	Value	Function	Remark
0x11	0x00	Crystal free run	bit[1:0]=b'00
0x12	0x08	SPDIF stop out when output mode change	
0x13	0x00	Output port de-jitter set to normal	bit[7:5]=b'000
0x14	0x40	Fading mode setting	bit[4:0]=h'00
0x30	0x23	SPDIF CDR Frequency detector	
0x31	0x19	SPDIF CDR phase detector gain	
0x39	0xF3	In/Out PLL bandwidth	bit[7:4]=h'F
0x3B	0x77	In/Out PLL offset	
0x40	0x02	Input PLL switch to high bandwidth mode	bit[4]=b'0
0x45	0x00	Output PLL gain setting to min	bit[3:2]=b'00
0x47	0xA4	Bypass check SPDIF CDR fine lock	bit[7] = b'1
0x4D	0x07	PCM volume shift gain SPDIF new coarse offset mode enable	Bit[5:4]=b'00 bit[1] = b'1
0x4E	0x77	In/Out PLL band width	
0x61	0x08	Digital OSC frequency fine tune to 50MHz	
0x62	0x01	select to use digital OSC	
0x09	0x00	Volume Left	
0x0A	0x00	Volume Right	
0x06	0x48	Disable output mute function	bit[7] = b'0

I2S Output port and Frequency setting

The I2S output port 1 can be configurated to master or slave output mode. Select one mode according to system application.

A. Master output on SRC mode 3 (any SRC mode is accept, see page 11 for detail.)

Address	Bit	Value	Function
0x04	6:4	0x03	SRC mode 3
0x05	3:0	--	Output freq. table selection on SRC mode 3. depends on spec to select one

B. I2S Slave output on SRC mode 0 (must set to SRC mode 0 when select to slave mode)

Address	Bit	Value	Function
0x04	6:4	0x00	SRC mode 0
0x05	6:0	--	Output freq. is control by external clock input (another I2S master device).

*Make sure POR1 is set to I2S slave mode.

If hardware POR 1 pin already config to master mode, it can use register to change the configuration again when system evaluation.

Address	Bit	Value	Function
0x4D	6	1	Inverse I2S slave mode setting

This setting is not recommand when production, the I2S's LRCK and BCLK signal might conflict due to there are two I2S master device on the same signal path.

Input Port select

Address	Bit	Value	Function
0x04	2:0	--	Dynamic select depends on system control

Advance function control

For more advance function control, please see the following description.

Hardware

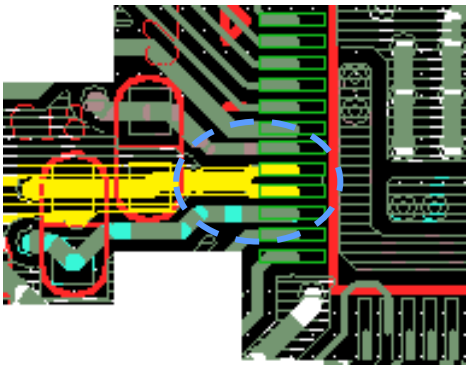
Schematic

Reference demo board schematic for detail.

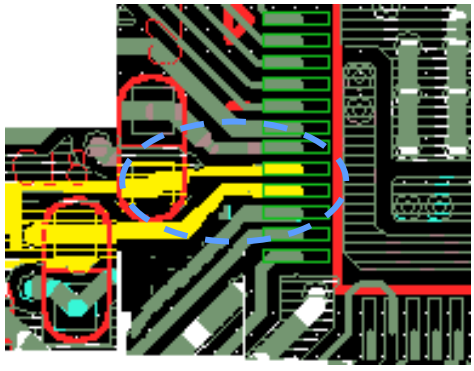
Layout Notice

There are 6 power input pins and each pin has its corresponding GND pin. To reduce the effect from power and ground noise, the bypass capacitor is required and near to pin as close as possible. These pins should connect to their bypass capacitor before connect to system ground evan there is another ground pin is near this pin.

Pin Name	Type	Pin No.		
		LQFP 48	QFN 32	
DVDD_12_CORE	Power	7	3	Group 1
DVSS_12_CORE	GND	8	4	
DVDD_33_PAD_0	Power	10	6	Group 2
DVSS_PAD_0	GND	9	5	
DVDD_33_PAD_1	Power	20	12	Group 3
DVSS_PAD_1	GND	21	13	
AVDD_12_LPLL	Power	29	18	Group 4
AVSS_12_LPLL	GND	28	17	
DVDD_33_PAD_2	Power	34	22	Group 5
DVSS_PAD_2	GND	35	23	
DVDD_33_PAD_3	Power	40	27	Group 6
DVSS_PAD_3	GND	41	28	



Short is not suggest on GND pin directly



Suggest layout design to separate two GND pin before bypass capacitor

Hardware Power on Latch (POR) control pin

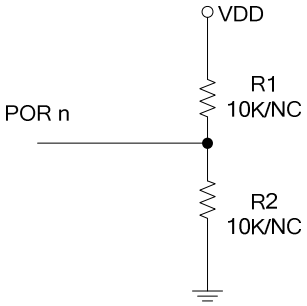
There are 5 POR pins on CT7302 serial chip for 3 functions definition. Use these 5 pins' signal level to define chip hardware characteristic. Each pin has to connect to VDD or GND pass through 10KΩ resistor depends on request. It latches the signal level status when chip is power on and internal reset period. Any signal level change is ignored after chip active.

Pin Name	Description	Function Table
POR_IN_1	POWER_ON_LATCH_DC[1] = SEL_I2S_TX_SLAVE_MODE	Select I2S1 output port is master or slave mode
POR_IN_3 POR_IN_4	POWER_ON_LATCH_DC[4:3] = SEL_XTAL[1:0]	Select Crystal frequency
POR_IN_5 POR_IN_6	POWER_ON_LATCH_DC[6:5] = I2C_ID[1:0]	I2C serial interface device ID selection

Each pin has internal pull low 120K ohm resistor.

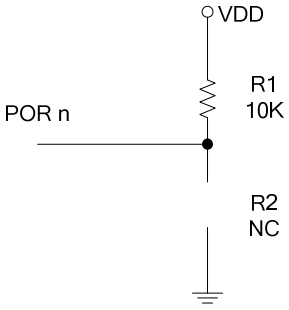
We suggest user reserve a 10K ohm resistor to VDD or GND for these pins to make sure chip can latch the correct user define value.

Suggest circuit for each POR pin

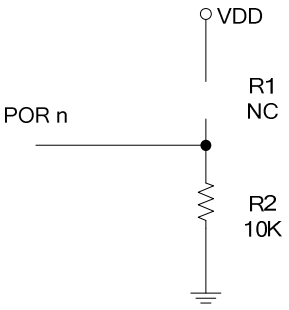


Use R1 / R2 to define each pin signal level when chip is power on.

POR = 1



POR = 0



I2S output slave mode:

Select I2S1 output port

No.	POR1	Definition
0	0	I2S output master mode
1	1	I2S output slave mode

Hardware Crystal:

Select current external crystal frequency

No	POR4	POR3	Definition
0	0	0	12.0000MHz
1	0	1	11.2896MHz
2	1	0	12.2880MHz
3	1	1	14.3180MHz

I2C Slave ID

Define chip I2C slave address

No	POR6	POR5	Definition
0	0	0	0x20
1	0	1	0x22
2	1	0	0x24
3	1	1	0x26

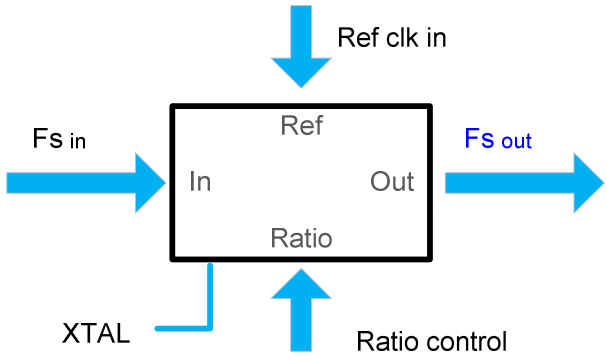
SRC Mode & Output Frequency

Mode Selection

- There are 7 different Sampling Rate Convert (SRC) control modes on CT7302 to change the audio output frequency.

SRC Mode	Output / Input Synchronous	Reference Clock	Reference Type	Ratio
0	X	ASRC pin	Fs	1
1	X	ASRC pin	Fs	N
2	X	ASRC pin	MCLK	N
3	X	XTAL	XTAL	LUT
4	√	Input Port	Fs	LUT
5	√	Input Port	Fs	N
6, 7	Bypass	-	-	-

There are 4 parameters relate with SRC mode: ***Input clock Fs in***, ***XTAL***, ***Refer clock in*** and ***index*** (or ***ratio***).

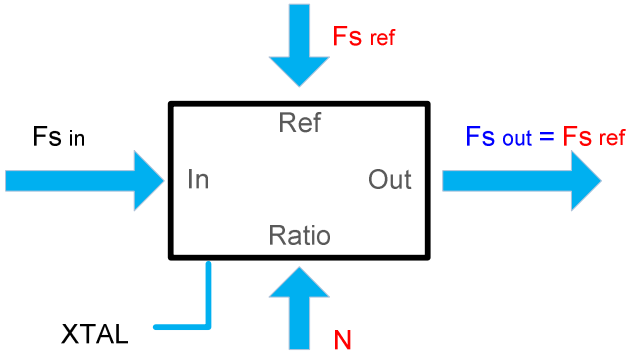


The output frequency is a combination of input frequency, Ref (external clock input) and Ratio (register setting) depends on SRC mode selection on Reg04[6:4].

SRC mode description

1. mode 0:

   The output frequency is same as Fs ref frequency on ASRC_REF_CLK_IN pin.



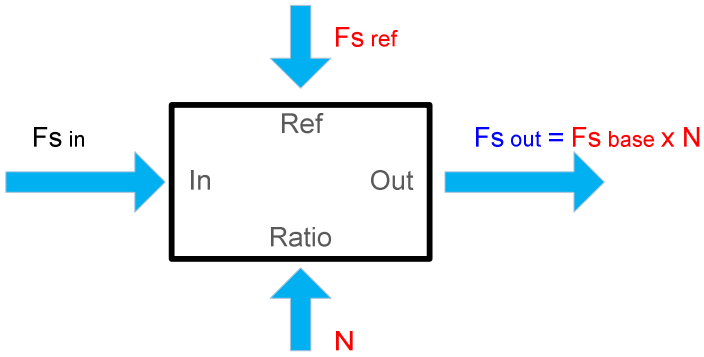
2. mode 1:

   The output frequency is synchronous to reference Fs clock (**Fs ref**) input on ASRC_REF_CLK_IN pin. Chip will calculate the base Fs (Fs base: 32K, 44.1K or 48K) automatic from **Fs ref** by divide 2^n.

   For example:

Reference Fs (input)	Base Fs
32K, 64K, 128K, 256K	32K
44.1K, 88.2K, 176.4K, 352.8K	44.1K
48K, 96K, 192K, 384K	48K

   The output frequency is Fs base * Output Ratio N.



3. mode 2:

   Similar to mode 1, the clock source on ASRC_REF_CLK_IN is mclk. The mclk should be 2^n * Fs base. Chip will calculate the base Fs by mclk/M that the parameter M is equal to 2^n. And the Fs base's Frequency range is between 30KHz to 50KHz. For example,

   The output frequency is Fs base * Output ratio N. Where N is one of {1, 2, 4, 8, 16} that select by OUTPUT_FREQ_SELECT[2:0].

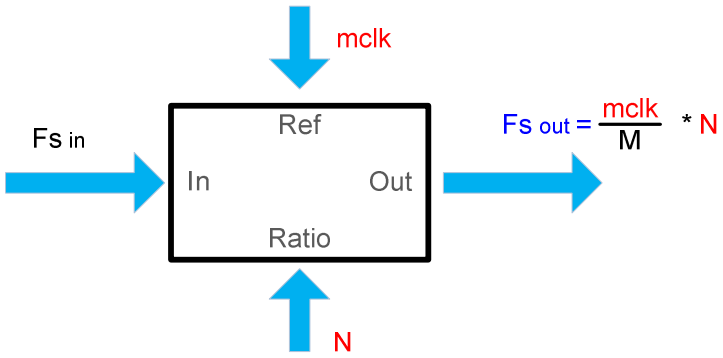
   For example,

   a. mclk = 11.2896MHz, ratio = 2

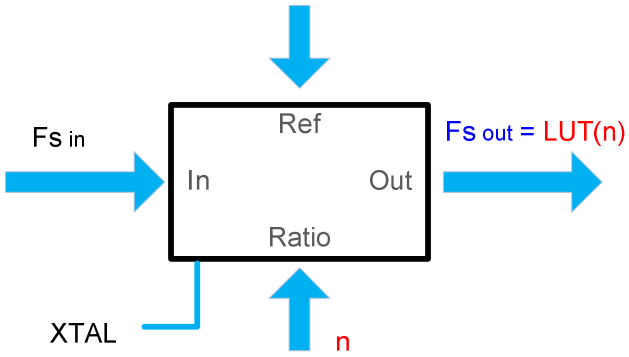
      → M = 2^8 = 256 (by chip algorithm) ➔ Fs is 44.1KHz

      output frequency is 44.1*2 = 88.2KHz

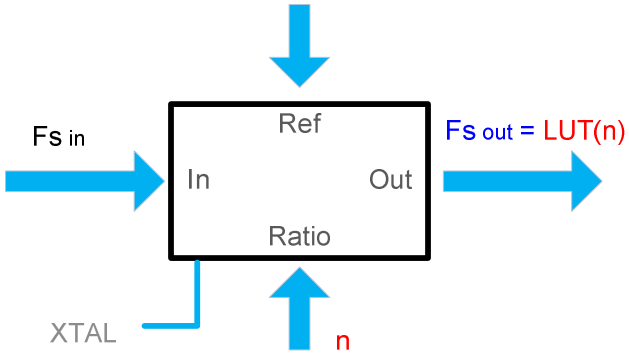
b. mclk = 24.5760MHz, ratio = 4
→ M = 2^9 = 512 (by chip algorithm) ➔ Fs is 48.0KHz
output frequency is 48.0*4 = 192KHz



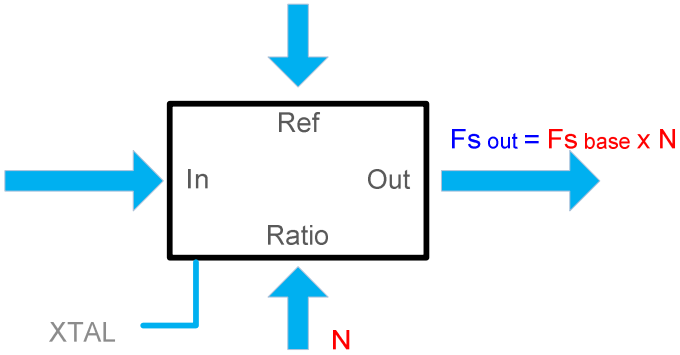
4. mode 3:
This is a pure asynchronous mode without any limit. User can select one of 15 output frequency any time from the list table. The reference clock source is XTAL and output is no related with input timing. This is suggested SRC mode for general system application.



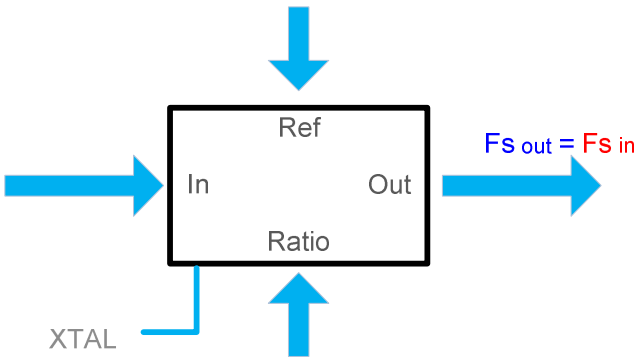
5. mode 4:
Similar to mode 3, user can select any output frequency from timing table. But the clock source is input channel. The input and output are synchronous.



6. mode 5:
   Similar to mode 1, but the clock source is input source clock. Chip will calculate the base Fs (Fs base) form Fs in. The output frequency is Fs base * Output Ratio N.



7. mode6, mode7:
   The output frequency is same as input and fully synchronous.



Output Frequency selection

According to SRC mode, there are 3 kind of output frequency selection:

1. Fix output:
   SRC mode is select to mode 0, 6, 7.
   The output frequency is same as input or Fs on ASRC pin. It can't be change on any condition or parameter.
2. Ratio control:
   SRC mode is select to mode 1, 2, 5.
   The output frequency is base on the fundamental frequency of input or Fs or MCLK on ASRC pin. Use Register 0x05[6:4] to select the ratio of output. The output frequency is equal to Fs base * ratio.
3. Look up table:
   SRC mode is select to mode 3, 4.
   Use Register 0x05[3:0] to select the output frequency directly. The final output frequency is same as this selection and no need to consider the other condition and setting.

SRC mode and Output frequency selection table

SRC mode and Output frequency selection table:

SRC Mode	Description	Output Frequency		
		Freq. Index Reg05[3:0]	Ratio Reg05[6:4]	Frequency
000	Synchronous to REFC_IN Fs input	-	-	Same as REFC_IN input clock
001	Synchronous to REFC_IN Fs input with ratio selector Fs output = Fs_{base} * N	-	000	1x Fs_{base} (32 / 44.1 / 48)
		-	001	2x Fs_{base} (64 / 88.2 / 96)
		-	010	4x Fs_{base} (128 / 176.4 / 192)
		-	011	8x Fs_{base} (256 / 352.8 / 384)
		-	100	16x Fs_{base} (512 / 705.6 / 768)
		-	others	reserve
010	Synchronous to REFC_IN MCLK input with ratio selector Fs output = Fs_{base} * N	-	000	1x Fs_{base} (32 / 44.1 / 48)
		-	001	2x Fs_{base} (64 / 88.2 / 96)
		-	010	4x Fs_{base} (128 / 176.4 / 192)
		-	011	8x Fs_{base} (256 / 352.8 / 384)
		-	100	16x Fs_{base} (512 / 705.6 / 768)
		-	others	reserve
011	Asynchronous, direct select target output frequency from index table Fs output = LUT(n)	0000	-	32 kHz
		0001	-	32 kHz
		0010	-	44.1KHz
		0011	-	48KHz
		0100	-	64 kHz
		0101	-	88.2 kHz
		0110	-	96 kHz
		0111	-	128 kHz
		1000	-	176.4 kHz
		1001	-	192 kHz
		1010	-	256 kHz
		1011	-	352.8 kHz
		1100	-	384 kHz
		1101	-	512 kHz
		1110	-	705.6 kHz
		1111	-	768 kHz

SRC mode and Output frequency selection table (cont.)

SRC Mode	Description	Output Frequency		
		Freq. Index Reg05[3:0]	Ratio Reg05[6:4]	Frequency
100	Synchronous to input port, direct select target output frequency from index table Fs output = LUT(n)	0000	-	32 kHz
		0001	-	32 kHz
		0010	-	44.1KHz
		0011	-	48KHz
		0100	-	64 kHz
		0101	-	88.2 kHz
		0110	-	96 kHz
		0111	-	128 kHz
		1000	-	176.4 kHz
		1001	-	192 kHz
		1010	-	256 kHz
		1011	-	352.8 kHz
		1100	-	384 kHz
		1101	-	512 kHz
		1110	-	705.6 kHz
		1111	-	768 kHz
101	synchronous to input with ratio selector Fs output = Fs_{base} * N	-	000	1x Fs_{base} (32 / 44.1 / 48)
		-	001	2x Fs_{base} (64 / 88.2 / 96)
		-	010	4x Fs_{base} (128 / 176.4 / 192)
		-	011	8x Fs_{base} (256 / 352.8 / 384)
		-	100	16x Fs_{base} (512 / 705.6 / 768)
		-	others	Reserve
110	BYPASS SRC	-		Fs output = Fs input
111	BYPASS SRC	-		Fs output = Fs input

DSD / PCM converter

Basic DSD to PCM converter

- This basic converter function provides DSD/DoP converter to PCM format. Output frequency is adjustable on this chip.

Both of the following 2 registers are set to “0” to disable the new conversion function and keep it on the basic converter mode.

Function	Address	Setting Value
New D2P enable	0x4D[0]	0: Disable New DSD to PCM converter
New P2D enable	0x59[0]	0: Disable PCM to DSD function.

The I2S or SPDIF output port can be configurated to DoP or PCM format depends on register setting. The output ports use the same setting and have the same output format when input source is DSD or DoP.

Function	Address	Setting Value
DoP/DSD converter	0x10[6]	When input source is DSD or DoP 0: DoP output 1: Convert to PCM output automatic.

- Output frequency setting on basic converter mode

  The output frequency can be set to fix mode or manual mode no matter its format is DoP or PCM. Fix mode means the output frequency is fixed and equal to input. The output frequency is adjustable when it select to manual mode only.

Function	**Address**	**Setting Value**
D2P Frequency mode	0x4C[3]	0: Output frequency Fix mode 1: Manual adjust output frquency
D2P Frequency ratio	0x4C[2:0]	Valid when Manual adjust mode (0x4C[3] = 1) 000~100 to different output ratio

Output register setting table:

1. Fix mode at Reg0x4C[3] = 0

   The output frequency is not adjustable and always same as DSD input. DSD and DoP is available on this mode.

Input	Output		
DSD/DoP	DSD	DoP (Reg10[6]=0)	PCM (Reg10[6]=1)
1x (2.8M)	Not Available	4xFs (176.4K)	1xFs (44.1K)
2x (5.6M)		8xFs (352.8K)	2xFs (88.2K)
4x (11.2M)		16xFs (705.6K)	4xFs (176.4K)

2. Manual mode at Reg0x4C[3] = 1

   The PCM format output frequency is selectable according to Reg0x4C[2:0] setting value. DSD output port and DoP format output on I2S or SPDIF port is no longer support at this mode.

Input	Output		
DSD/DoP	DSD/DoP	Reg4C[2:0]	PCM (Reg10[6]=1)
Any mode	Not Available	000	1xFs (44.1K)
		001	2xFs (88.2K)
		010	4xFs (176.4K)
		011	8xFs (352.8K)
		100	16xFs (705.6K)

Advance DSD to PCM (D2P) and PCM to DSD (P2D) converter

- Advance DSD to PCM converter. (CT7302 all serial only)

  The advance DSD (DoP) to PCM converter function is enabled when following register is set.

Function	Address	Setting Value
New D2P enable	0x4D[0]	1: Enable New DSD to PCM converter

I2S and SPDIF output port can be set to any PCM format freqency by Reg05[6:4] or Reg05[3:0] according to which SRC mode you select. The setting is same as general PCM format input.

Input	Output Freq. Configuration		Output Freq
DSD/DoP/PCM	Reg05[6:4] SRC mode 1, 2, 5	Reg05[3:0] SRC mode 3, 4	PCM
PCM 32K~768KHz DSD 1x ~ 8x DoP 1x ~ 4x	000	0000, 0001, 0010, 0011	1xFs base
	001	0100, 0101, 0110	2xFs base
	010	0111, 1000, 1001	4xFs base
	011	1010, 1011, 1100	8xFs base
	100	1101, 1110, 1111	16xFs base

Fs base is mean the fundamental audio sampling rate: 32KHz, 44.1KHz or 48KHz

- Advance PCM to DSD converter. (CT7302P, CT7302C only)

  The advance PCM to DSD converter function is enabled when following register is set.

Function	Address	Setting Value
New P2D enable	0x59[0]	1: Enable New PCM to DSD converter

There are two I2S/DSD output ports on this serial chip, both of them can be set to I2S (PCM or DoP) or DSD format by register configuration.

Function	Address	Setting Value
I2S/DSD port 0	0x59[5]	output port format and pin definition 0: I2S port 1: DSD port
I2S/DSD port 1	0x59[4]	output port format and pin definition 0: I2S port 1: DSD port

SPDIF and I2S output port can be configurated to DoP or PCM format by register 0x59[1] when PCM to DSD function is enabled.

Output Format control summary

Output Format	Address	Setting Value
I2S PCM	0x59[5:4]	0: I2S port output format definition, see above
	0x59[1]	0: PCM output
I2S DoP	0x59[5:4]	0: I2S port output format definition, see above
	0x59[1]	1: DoP output
DSD format	0x59[5:4]	1: I2S port output format definition, see above
	0x59[1]	-

DSD/DoP output frequency can be configuration to 1x, 2x, 4x and 8x Fs by register Reg59[3:2]. But this freqency is limited and can not exceed PCM format output frequency.

PCM Output Freq.	DSD / DoP Output configuration		
	Reg59[3:2]	DSD *1	DoP*2
1xFs base	00 (DSD 1x mode)	DSD 1x / 64xFs base	DoP 1x / 4Fs base
	01 (DSD 2x mode)		
	10 (DSD 4x mode)		
	11 (DSD 8x mode)		
2xFs base	00 (DSD 1x mode)	DSD 1x / 64xFs base	DoP 1x / 4Fs base
	01 (DSD 2x mode)	DSD 2x / 128xFs base	DoP 2x / 8Fs base
	10 (DSD 4x mode)		
	11 (DSD 8x mode)		
4xFs base	00 (DSD 1x mode)	DSD 1x / 64xFs base	DoP 1x / 4Fs base
	01 (DSD 2x mode)	DSD 2x / 128xFs base	DoP 2x / 8Fs base
	10 (DSD 4x mode)	DSD 4x / 256xFs base	DoP 4x / 16Fs base
	11 (DSD 8x mode)		
8xFs base 16xFs base	00 (DSD 1x mode)	DSD 1x / 64xFs base	DoP 1x / 4Fs base
	01 (DSD 2x mode)	DSD 2x / 128xFs base	DoP 2x / 8Fs base
	10 (DSD 4x mode)	DSD 4x / 256xFs base	DoP 4x / 16Fs base
	11 (DSD 8x mode)	DSD 8x / 512xFs base (DSD+PCM mode only)	-

** Fs base is mean the fundamental audio sampling rate: 32KHz, 44.1KHz or 48KHz

*1 DSD 1x = 64xFs base. When PCM output frequency is 44.1K, the DSD frequency is 44.1K x 64 = 2.822MHz

DSD 2x = 128xFs base. When PCM output frequency is 192K, Fs base is 48K.

The DSD frequency is 48K x 128 = 6.144MHz

*2 DoP 1x = 4xFs base. When PCM output frequency is 44.1K, the DoP frequency is 44.1K x 4 = 176.4KHz

Input / Output port

Input source select

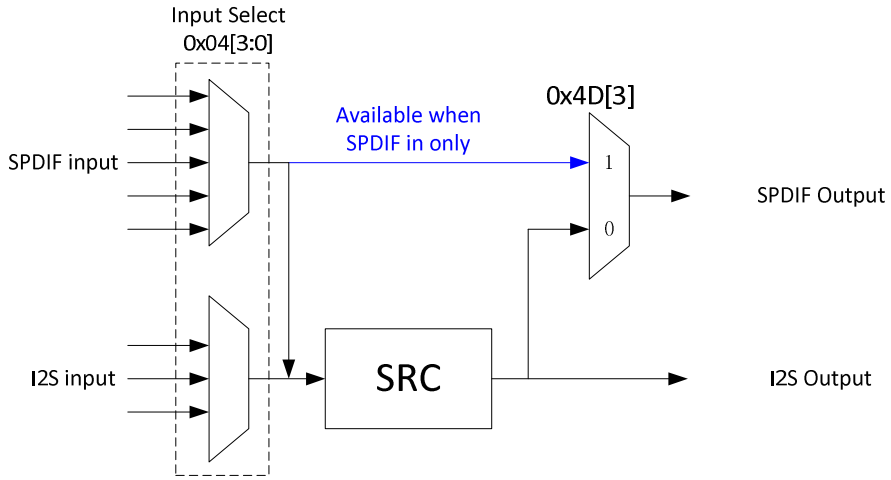
There are 5 SPDIF (input channel 0 ~ 4) and 3 I2S/DSD input ports (input channel 5, 6 and 7) on CT7302 serial chip. Some input sources are not available on CT5302 serial chip. Select one of them to chip internal SRC process.

Function	Address	Setting Value
Input Channel select	0x04[2:0]	Select 1 of 8 input port. 0: SPDIF IN-0 1: SPDIF IN-1 2: SPDIF IN-2 3: SPDIF IN-3 4: SPDIF IN-4 5: I2S IN-0 6: I2S IN-1 7: I2S IN-2

The SPDIF output data can be selected from current SPDIF input port or after CT7302's internal SRC process. That is a useful function to bypass SPDIF input signal to output port directly when connect the same signal to next device.

Function	Address	Setting Value
SPDIF directly output	0x4D[3]	0: normal with SRC 1: direct passthrough selected input

Simple function block of SPDIF bypass mode:



I2S Input port format setting

The 3 I2S input ports can be configed to I2S or DSD format manual by register.

Function	Address	Setting Value
Channel 7 input format I2S IN-2 / DSD IN-2	0x4C[7]	0: Pin and format define as I2S port 1: Pin and format define as DSD port
Channel 6 input format I2S IN-1 / DSD IN-1	0x4C[6]	0: Pin and format define as I2S port 1: Pin and format define as DSD port
Channel 5 input format I2S IN-0 / DSD IN-0	0x4C[5]	0: Pin and format define as I2S port 1: Pin and format define as DSD port

Another simple way is set all of these 3 ports to auto detect mode

Function	Address	Setting Value
Auto I2S/DSD detect	0x4C[4]	0: manual mode, define by Reg4C[7:5] 1: Auto detect mode (default)

Read Reg7A[3] to get current select port is I2S or DSD format input when set to auto detect mode.

Function	Address	Setting Value
I2S/DSD format detect	0x7A[3]	0: I2S 1: DSD

Input Status detect

1. Input signal clock status and input frequency report.
   Use Reg8E[1:0] to report the selected input port clock status. The indicate bit is set when SPDIF or I2S is stable and valid.

Function	Address	Get Value
SPDIF input status	0x8E[0]	0: no input signal 1: normal → CDR locked
I2S input status	0x8E[1]	0: no input signal 1: normal → Input locked

The following register can report the input frequency directly when selected input channel is locked.

Function	Address	Get Value
Input frequency	0x89[3:0]	Index for input freq. table

The register indicates current input frequency. All format include DSD, DoP and PCM are transferred to PCM frequency automatically.
This report value is calculated by chip internal PLL according to XTAL frequency setting. The XTAL frequency should match to hardware POR (#3, #4) configuration value.

2. Input format detect

I2S and SPDIF input can support PCM or DoP input format and always convert PCM automatic. To get current input format

Function	Address	Get Value
I2S DOP in	0x77[5]	0: non DoP 1: DoP signal input on I2S
SPDIF DOP in	0x77[4]	0: non DoP 1: DoP signal input on SPDIF

3. Input signal data length detect

Function	Address	Get Value
I2S 32bit data in	0x77[7]	0: non 32bit 1: input data rate format is 32 bit
SPDIF 32bit data in	0x77[6]	0: non 32bit 1: input data rate format is 32 bit

4. Input Data valid

Report the input data keeps at zero or not for a period of setting timing. Some audio source e.g. CD player

Function	Address	Get / Set Value
Input data zero flag	0x77[1]	0: Input data is non zero 1: input data stay at zero more than set sample
Input data zero count	0x15[7:0]	Input zero data samples count threshold for flag

5. Input Data silence detect

To detect current input data level, this chip provides a flag for user to get the input signal is lower than the threshold for a period.

Function	Address	Get Value
Detect Length	0x60[6:4]	Detect timer selection Delay timer to set the silence bit when input data level is keep low
Detect active sample	0x60[2:0]	Active data bit count threshold How many bits (MSB) no data input to trigger silence. 0: 14bit easy, 7: 32bit difficult
Silence detect flag	0x7A[7:5]	Report silence input data is low than threshold bit 7: R and L channel bit 6: Right channel bit 5: Left channel

6. I2S input format selection

   There are several different transfer formats on I2S data spec. CT7302 can support standard and left justified format on RX and TX port. For System application, user might need have different setting on input and output port.

Function	Address	Set Value
I2S RX format	0x06[4]	0: Standard format 1: Left justified

7. Low frequency input patch

   CT7302 serial support input range from 32K to 768K (depends on chip selection), that is enough for general audio application. But for some special source for example Bluetooth, the output frequency is lower to 8KHz.

   For this low frequency input signal, set the following register to multiply the input to 4 times for chip processing.

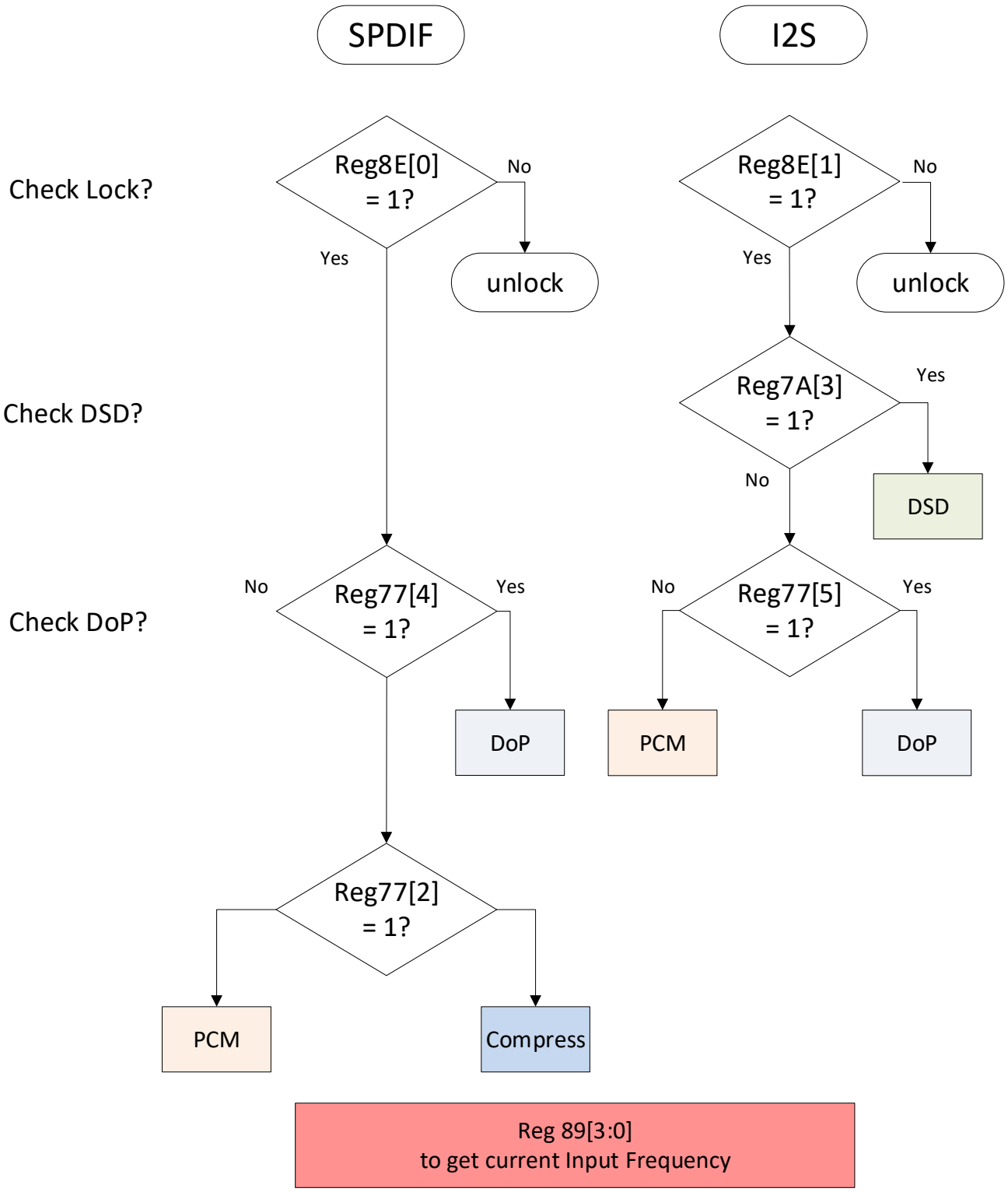
Function	Address	Set Value
I2S input low frequency support	0x4F[6]	Lower input from I2S 0: normal 1: detect frequency is input *4
SPDIF input low frequency support	0x4F[5]	Lower input from SPDIF 0: normal 1: detect frequency is input *4

8. Non PCM format (compress data) input from SPDIF port

Function	Address	Set Value
SPDIF non pcm input detect	0x77[2]	Lower input from I2S 0: normal 1: non pcm input
SPDIF non pcm data passthrough	0x07[2]	SPDIF non-pcm output data setting 0 = pass non-pcm data 1 = mute data

Input Format and Frequency detection procedure

1. Check register report input format and status depends on current selected port.



2. Check input frequency:
   Read register 0x89

Register 0x89	PCM	DoP	DSD
0x00 / 0x01	32K	DoP64 (Fs=32K)	DSD64 (Fs=32K)
0x02	44.1K	**DoP64 (Fs=44.1K)**	**DSD64 (Fs=44.1K)**
0x03	48K	DoP64 (Fs=48K)	DSD64 (Fs=48K)
0x04	64K	DoP 128 (Fs=32K)	DSD128 (Fs=32K)
0x05	88.2K	**DoP128 (Fs=44.1K)**	**DSD128 (Fs=44.1K)**
0x06	96K	DoP 128 (Fs=48K)	DSD128 (Fs=48K)
0x07	128K	DoP 256 (Fs=32K)	DSD256 (Fs=32K)
0x08	176.4K	**DoP256 (Fs=44.1K)**	**DSD256 (Fs=44.1K)**
0x09	192K	DoP 256 (Fs=48K)	DSD256 (Fs=48K)
0x0A	256K	NA	DSD512 (Fs=32K)
0x0B	352.8K	NA	**DSD512 (Fs=44.1K)**
0x0C	384K	NA	DSD512 (Fs=48K)
0x0D	512K	NA	NA
0x0E	705.6K	NA	NA
0x0F	768K	NA	NA

Typical DSD/DoP signal frequency is base on 44.1K. So the standard input clock will be 2.822MHz/5.644MHz/11.288MHz when DSD in.

Output port format setting

1. I2S output slave mode.

   CT7302 I2S0 port provides slave mode output selection for user application on system design. The default operation is configed by chip hardware Power On Latch (POR #1). But it also can adjust by register again after chip is power on. The following register can inverse the POR setting again when it is set.

   The SRC mode (Reg04[6:4]) must select to mode 0 when use slave mode.

Function	Address	Setting Value
Inverse I2S slave mode setting	0x4D[6]	0: same as POR config mode 1: Inverse setting

2. I2S output format selection

Function	Address	Set Value
I2S TX format	0x06[5]	0: Standard format 1: Left justified

3. 32 bit format output

Function	Address	Setting Value
I2S 32 bit output	0x06[3]	0: 24 bit output 1: 32 bit output
SPDIF 32 bit output	0x06[2]	0: 24 bit output 1: 32 bit output

4. DSD output data L/R swap

   CT7302P and CT7302C provide PCM to DSD converter

Function	Address	Setting Value
DSD data swap	0x5A[5]	0: normal 1: swap

Volume Control

General Volume control

Function	Address	Setting Value
Mute	0x06[7]	0: Normal output 1: Mute all output
Sync Right/Left channel Volume Control	0x07[0]	0: independent 1: Right equal to Left, Right control is disabled.
Left channel Volume control	0x09[7:0] 0x08[3:0]	12 bit volume control of left channel, each step is 0.03125db.
Right channel Volume control	0x0A[7:0] 0x08[7:4]	12 bit volume control of right channel, each step is 0.03125db. Valid when independent control bit is set.
Volume Gain Control	0x4D[5:4]	PCM volume control shift gain setting 00 = +0dB 01 = +6dB 10 = +12dB 11 = +18dB

The final PCM output volume gain will be Gain setting (Reg4D[5:4]) + Volume control (12bit).

For example,

a. Volume control set to 0x180 0x180 (hex) = 384 (dec) → 384 * 0.03125 = -12.0dB

b. Volume gain set to 10 10 → +12dB

c. The total volume control output is -12dB + 12dB = 0dB

DSD to PCM volume compensate

Most software or device will decrease 6dB before converter PCM format to DSD to avoid the signal is saturated and clipped. It should compensate the data to original level when this DSD data converter to PCM format.

Function	Address	Setting Value
DSD to PCM compensate	0x4D[2]	0: 0dB 1: +6dB

Chip will automatic compensate 6dB when this bit is set and input DSD/DoP converter to PCM format output.

PCM to DSD converter control

The DSD output volume can be adjusted independent when PCM to DSD converter function is enabled. It also can follow current general volume control.(CT7302P, CT7302C only)

Function	Address	Setting Value
Volume control independent	0x5A[2]	PCM to DSD volume control mode setting 0: independent 1: follow PCM volume control
Mute DSD	0x5A[4]	Mute volume when PCM to DSD converter
Sync Right/Left channel Volume Control	0x5A[3]	PCM to DSD volume control mode setting 0: independent 1: right channel is equal to left channel
Left channel Volume control	0x5C[7:0] 0x5B[3:0]	12 bit volume control of left channel, each step is 0.03125db.
Right channel Volume control	0x5D[7:0] 0x5B[7:4]	12 bit volume control of right channel, each step is 0.03125db. Valid when independent set.
Volume Gain Control	0x5E[5:4]	PCM to DSD gain 00 = +0dB 01 = +6dB 10 = +12dB 11 = +18dB

System application control

IRQ

There are several input, output and IC internal status change can be detected by chip and response to interrupt pin immediately. User can connect this pin to system MCU interrupt input port. And get more information from the relate register at Address 0x00 to 0x03 at the same time. The individual IRQ function also can be disabled by set the mask bit.

Due to CT7302 can auto mute the output volume when input signal is unstable or change and recovery it after the signal comes back. The response time is faster than MCU's process time, users can ignore the IRQ function to reduce MCU's system control loading.

SPDIF Channel status

According to IEC60958-3 standard, there are 24 bytes in SPDIF channel status can be used for transmit data or information to receiver. CT7302 open 5 byte for user to read on receiver side and set on transmitter side.

Function	Address	Value
TX Channel status	0x14[6]	0: use register 0x0B~0x0F setting value 1: use the data from SPDIF RX port
TX Channel status Setting Value	0x0F[7:0] | 0x0B[7:0]	5 byte setting value for include to SPDIF transmit port
RX Channel status	0x76[7:0] | 0x72[7:0]	Get 5 byte SPDIF input port channel status value

Power Codntrol

1. Power saving

To reduce power consumption, the output port or clock can be disabled when they are unused.

Function	Address	Setting Value
Ref Clock output	0x10[4]	0: Normal output 1: Disable Reference clock output and stop at 0
SPDIF output	0x10[3]	0: Normal output 1: Disable SPDIF output and stop at 0
I2S1 output	0x10[2]	0: Normal output 1: Disable I2S1 output and stop at 0
I2S0 output	0x10[1]	0: Normal output 1: Disable I2S0 output and stop at 0
I2S mclk output	0x10[0]	0: Normal output 1: Disable I2S mclk output and stop at 0

For system application, the output pin might keep at low or tri-state when power down or power saving mode depends on peripheral circuit design.

Function	Address	Setting Value
SPDIF TX stop mode	0x12[7]	0: stop at low 1: tri-state
I2S1 TX stop mode	0x12[6]	0: stop at low 1: tri-state
I2S0 TX stop mode	0x12[5]	0: stop at low 1: tri-state
I2S MCLK stop mode	0x12[4]	0: stop at low 1: tri-state

2. Power down

Set “Power down all” bit register will let chip into deep power saving mode. The “XTAL free run” setting can keep XTAL clock continue output when chip is power down for the other chip at system if they use the same clock system.

The other power modes describe at register 0x11 are test mode for chip designer.

Function	Address	Get Value
Power down all	0x11[7]	0: normal 1: power down all chip
XTAL free run	0x11[0]	0: normal 1: keep XTAL active at any power down state.

System Reset

There are several reset sources on CT7302 serial chip.

1. Hardware power on reset:

   Chip hardware reset automatic when system power 1.2V and 3.3V are stable and ready.

   The reset signal trigger again if any one of these two power drop and recover again.

2. Digital reset by register. 0x9F

Function	Address	Setting Value
Reset	0x9F[1]	1: Reset chip digital block.
Reset All chip digital	0x9F[0]	1: Reset all chip digital block, the register value is also clear to chip power on default value.

3. Analog PLL reset by register

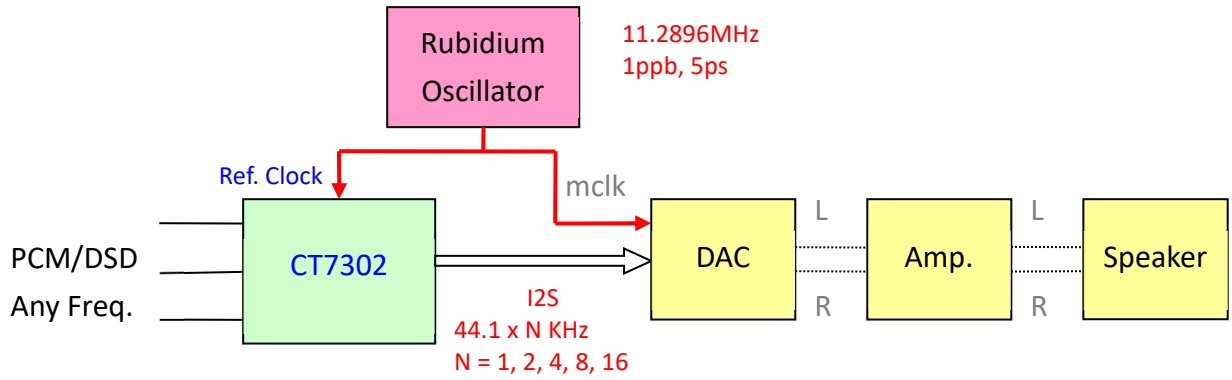
Function	Address	Setting Value
Input LPLL reset	0x2B[7]	0: Normal 1: Reset input LPLL.
MPLL reset	0x2B[3]	0: Normal 1: Reset MPLL.

Appendix

Low jitter output application system

The general IC output clock jitter on a typical COMS process is about 100 ps. That is suitable for most general application. But for some Hi-End Audio system, it might need an ultra high precision clock system with low jitter MCLK output to DAC to enhance audio performance.
For this requirement, CT7302 serial chip provide an output SRC mode to sync with the external precision reference clock at SRC mode 2. The I2S output BCLK / DATA / LRCK is sync to reference clock input at this mode. The MCLK for DAC is connected to high precision Rubidium Atomic clock source directly. So it can get better performance if this DAC need a good enough MCLK.

The application function block is shown as below:



The ultra high precision rubidium clock is send to CT7302 and DAC chip at the same time. CT7302 calculate the base Fs and get 11.2896M/256 = 44.1K result. The output frequency can be 44.1*N KHz and the data is sync to reference clock.