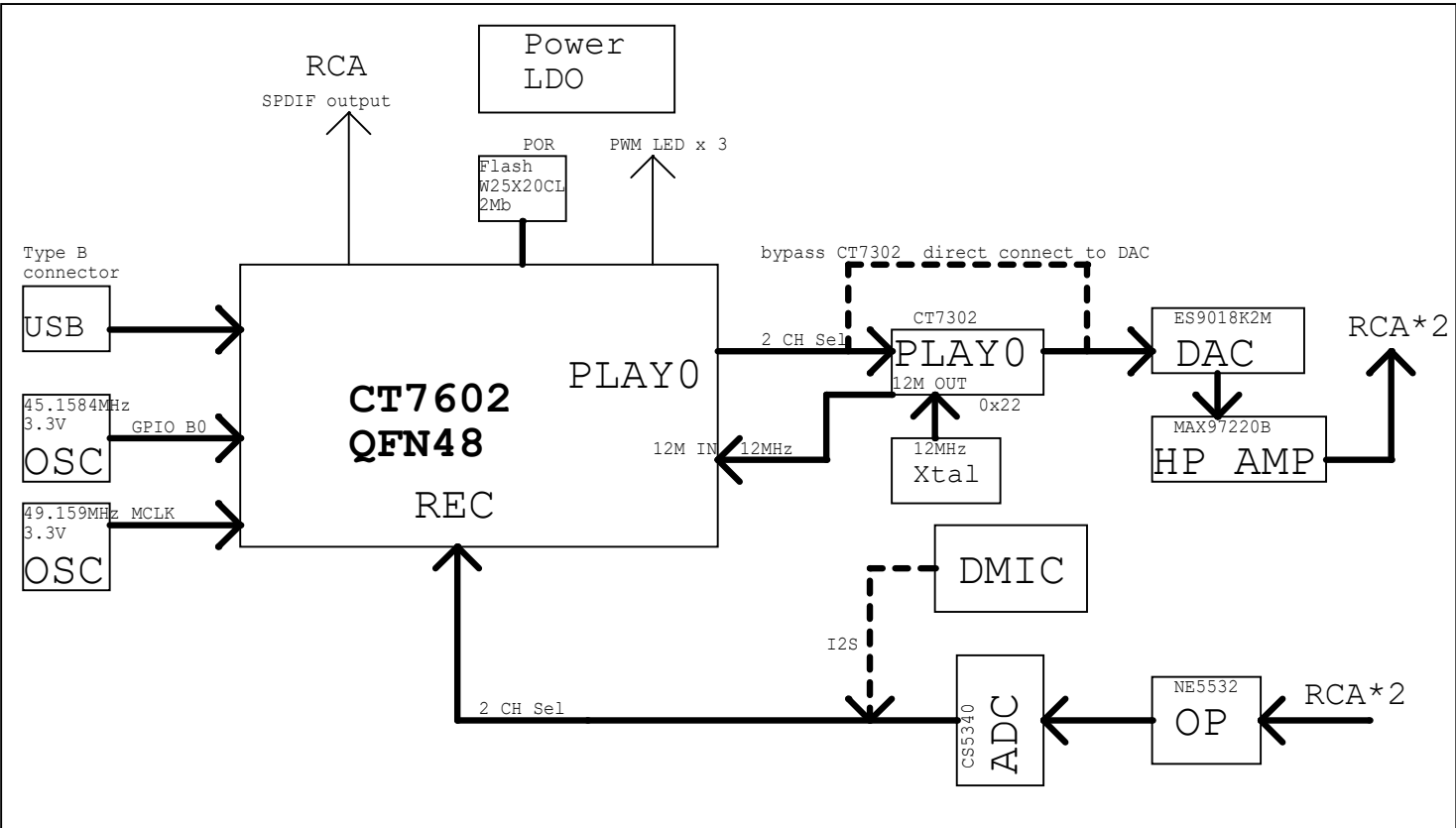
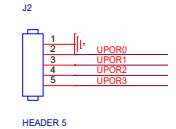
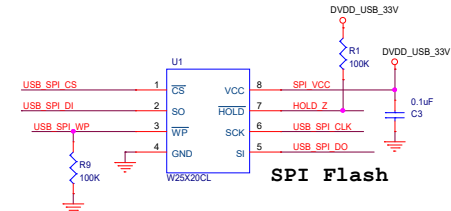
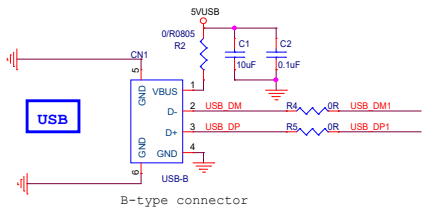
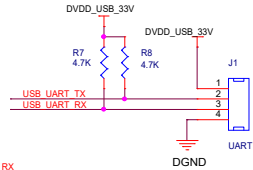
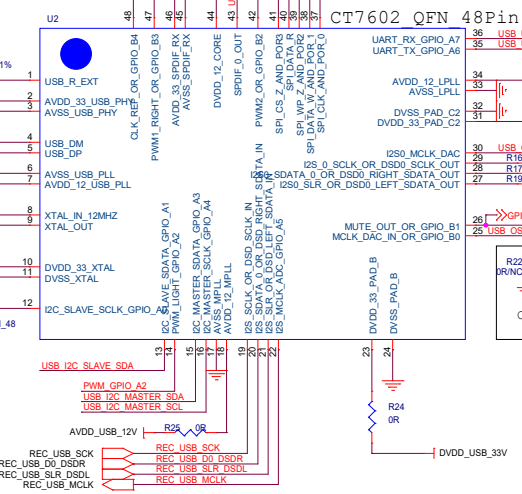






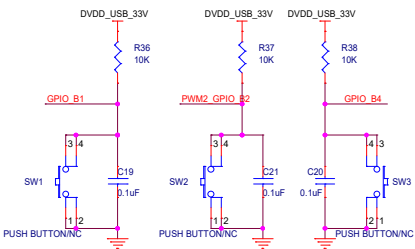
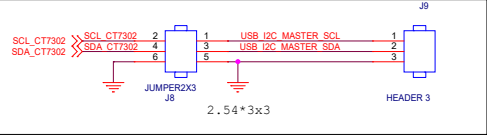
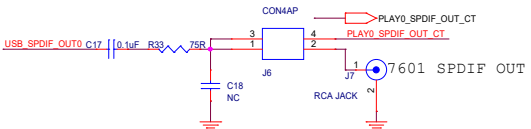
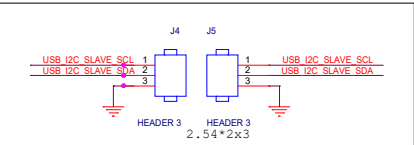
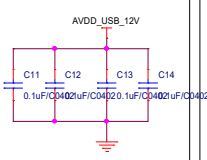
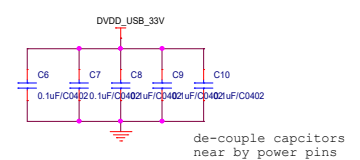
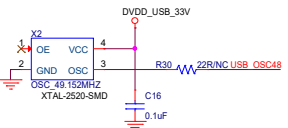
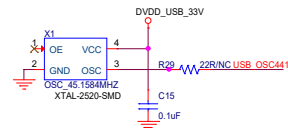
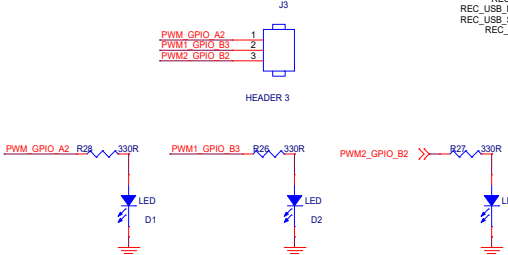
POR *4bit(WP reserved)



Play 0 output port

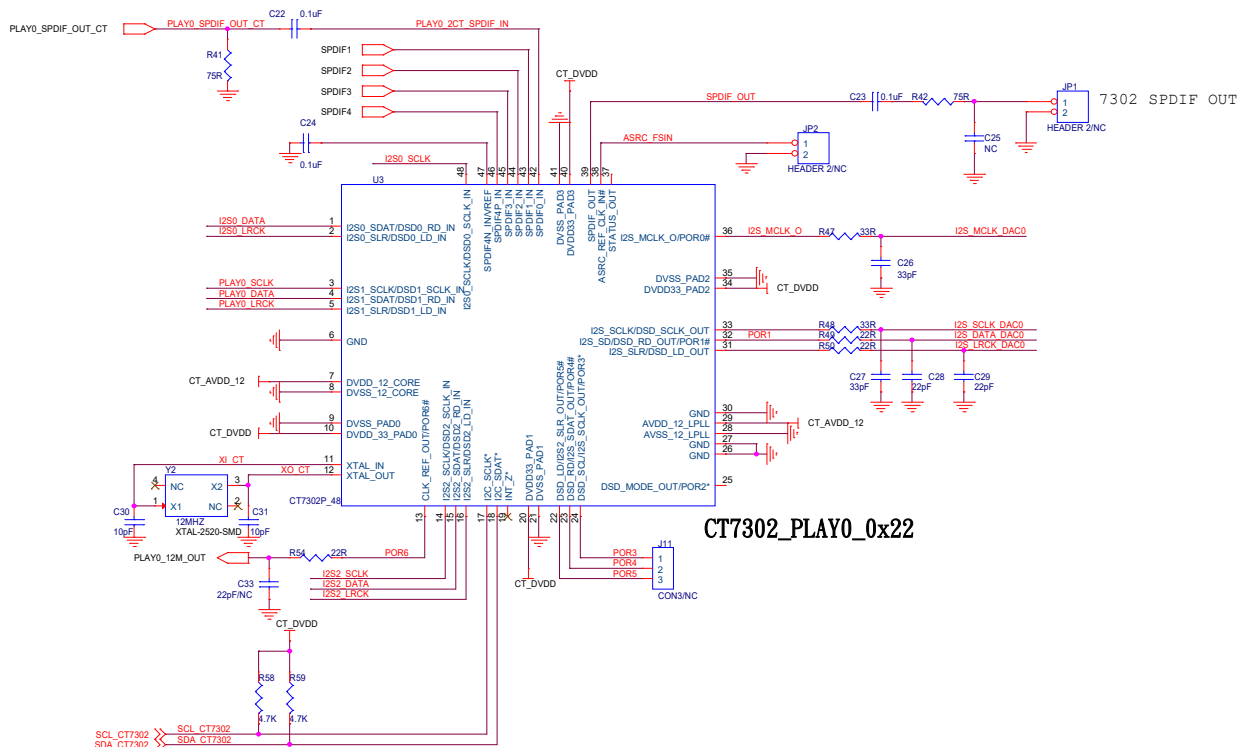
- USB PLAY0 MCLK
- USB PLAY0 SCK
- USB PLAY0 SLR_DSOL

REC input port



VOL- Start VOL+

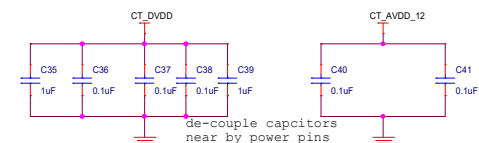
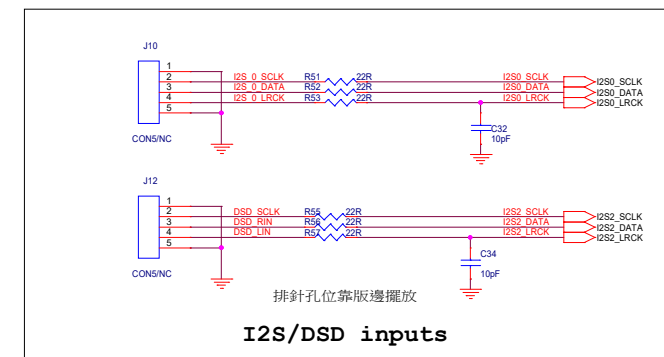
Title			
<CT7602_LQFP_48pin>			
Size	Document Number		Rev
	<Doc>		
Date:	Monday, November 28, 2022	Sheet	2 of 6



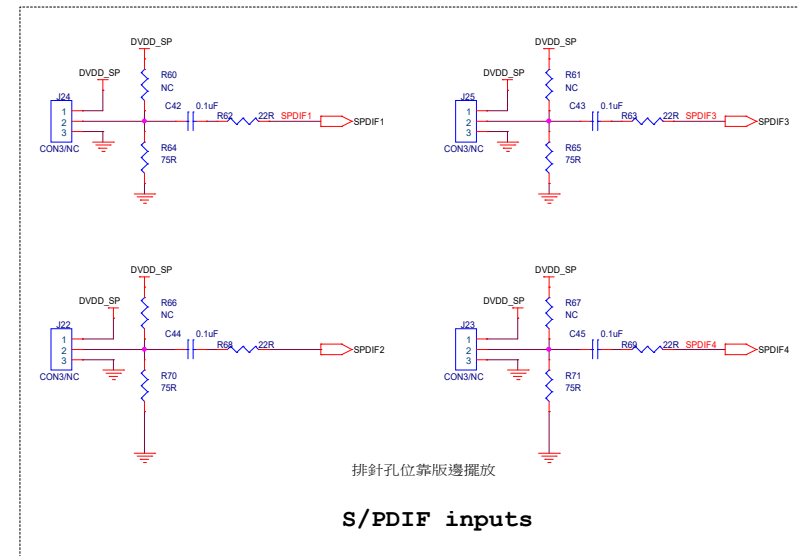
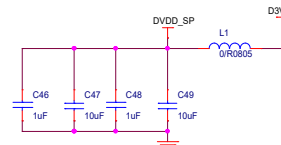
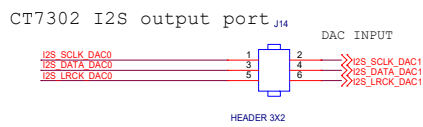
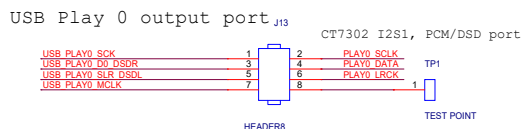
Power On Latch
POR1# : I2S Tx Salve/Master
0/1 (Master/Salve)

POR4#-3# : X'tal
00 (12M) 01 (11.2896M)
10 (12.288M) 11 (14.318M)
POR6#-5# : I2C ID
00 (x20) 01 (x22)
10 (x24) 11 (x26)

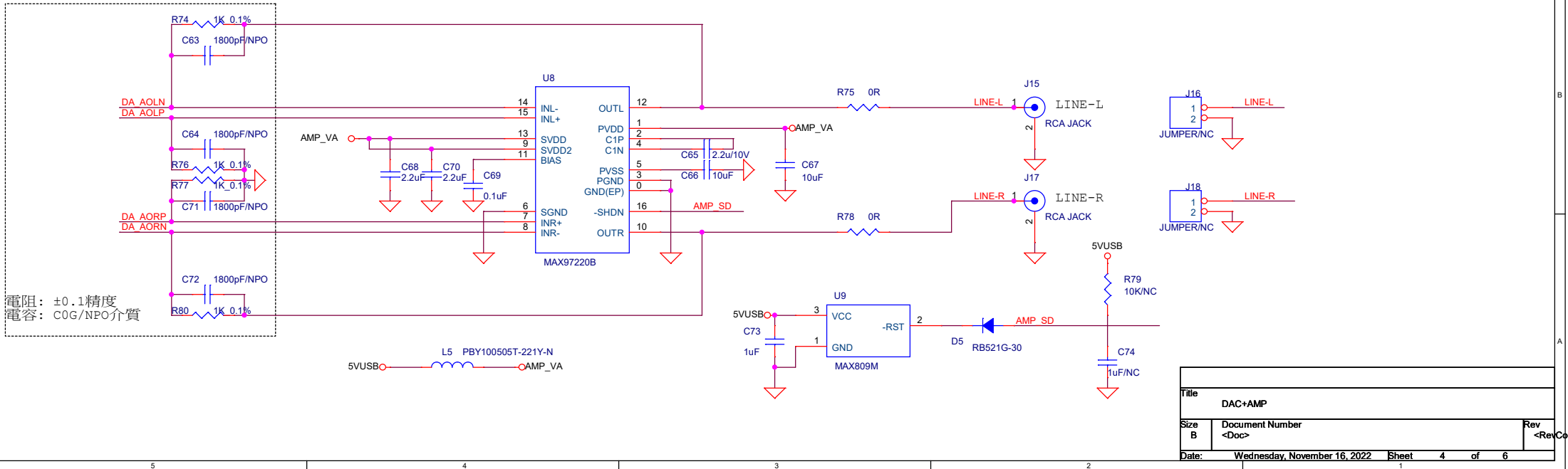
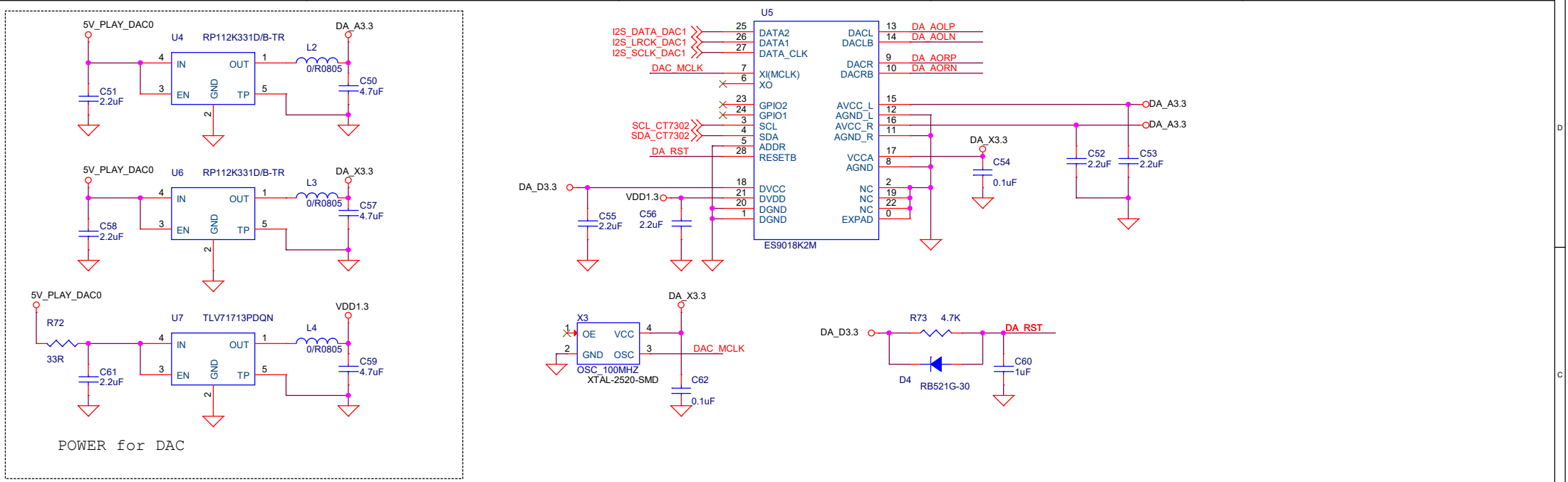
H/W configuration (POR setting)

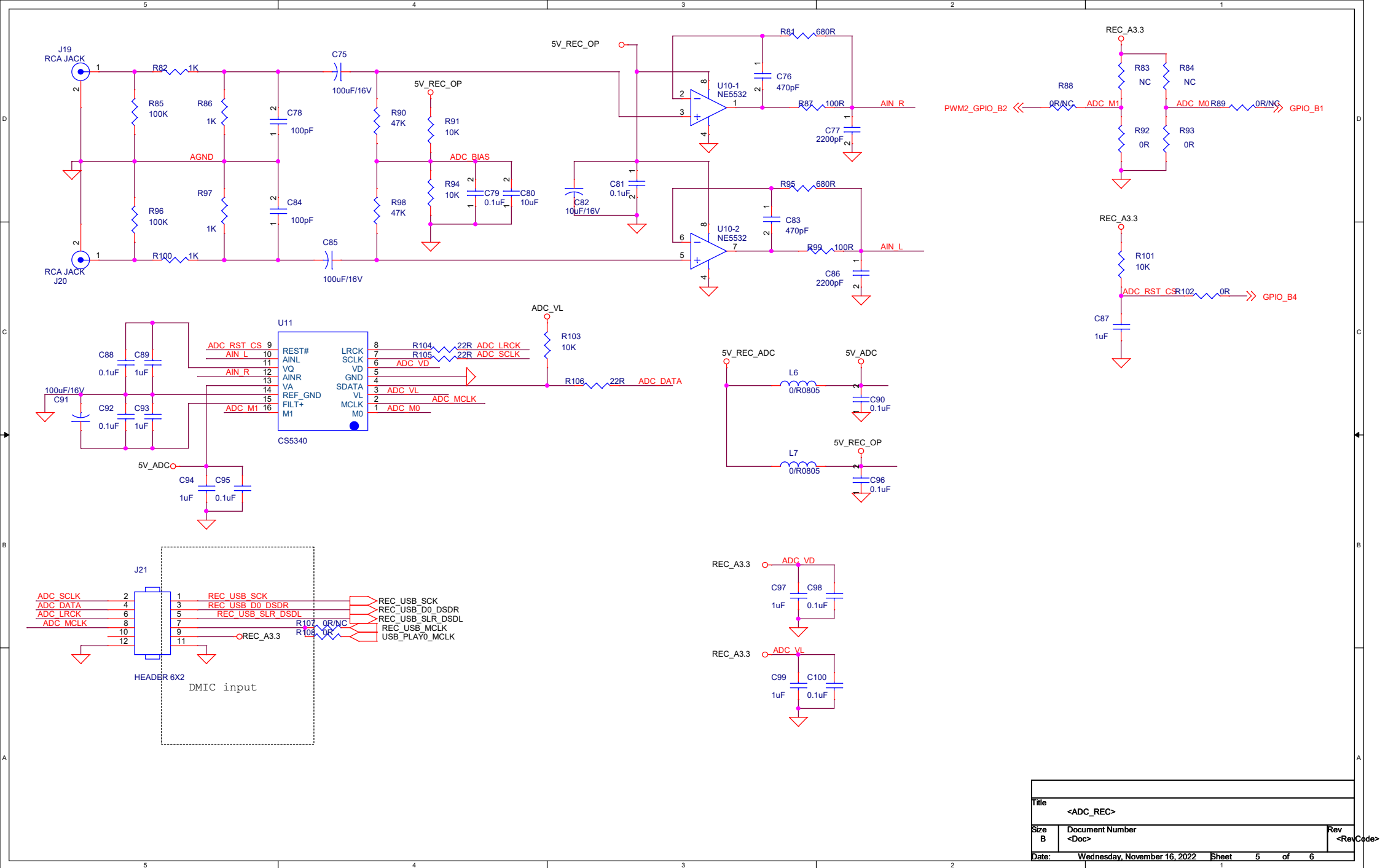


USB_PLAY0_MCLK
USB_PLAY0_SCK
USB_PLAY0_D0_DSOR
USB_PLAY0_SLR_DSOL

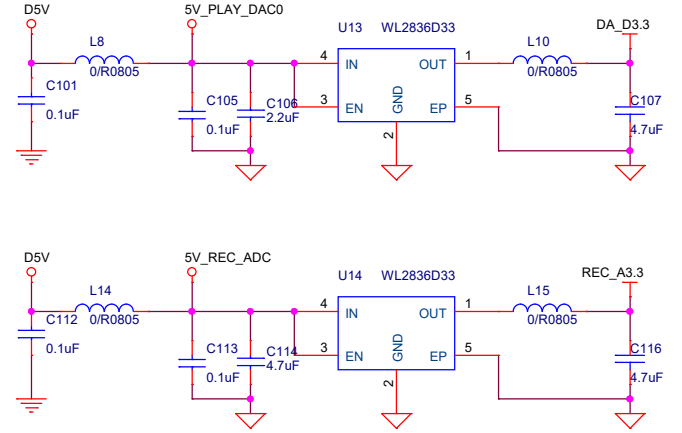
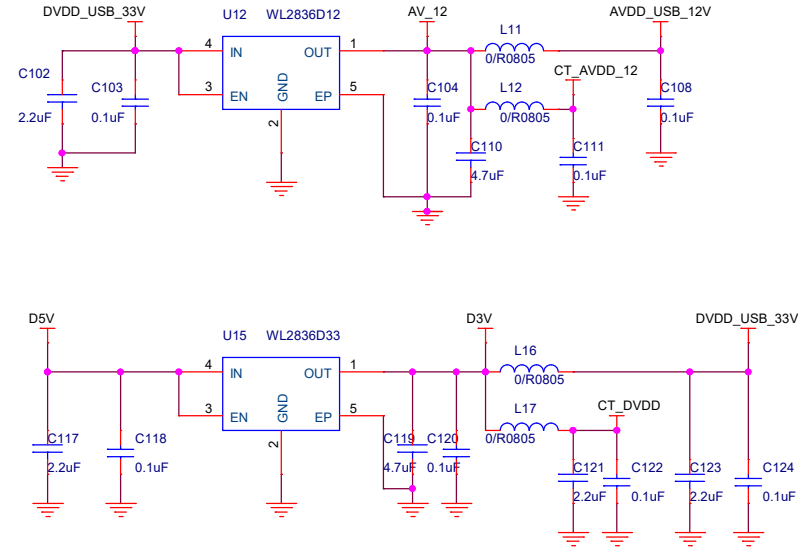
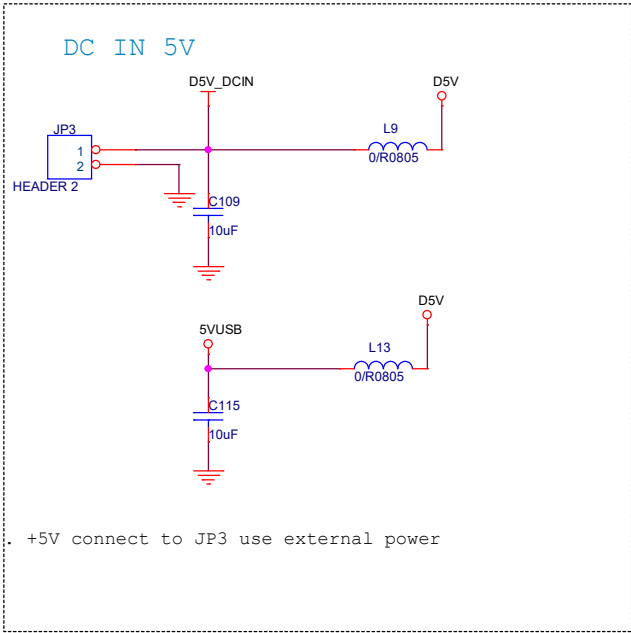


Title					
<CT7302_PLAY0>					
Size	Document Number				Rev
C	<Doc>				<Rev Code>
Date:	Wednesday, November 16, 2022		Sheet	3	of 6

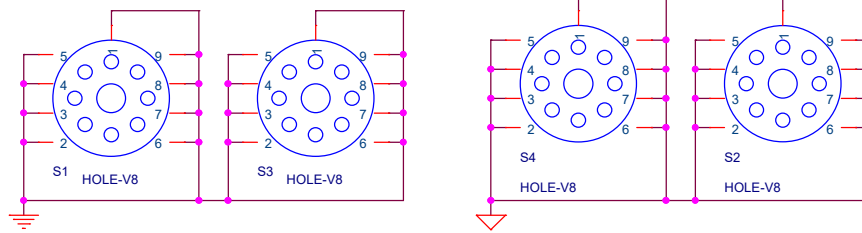
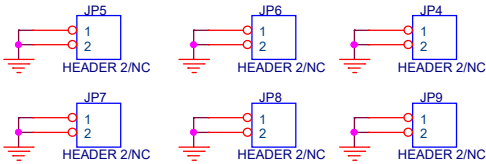
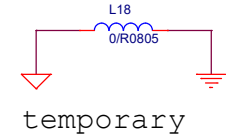




Title			<ADC_REC>		
Size	Document Number				Rev
B	<Doc>				<RevCode>
Date:	Wednesday, November 16, 2022				Sheet 5 of 6



Power for CT7601 & CT7302s



Title			<POWER>
Size	Document Number	Rev	
B	<Doc>	<RevCode>	
Date:	Wednesday, November 16, 2022	Sheet	6 of 6